Preventing Output Voltage Overshoot During VIN Transitions on the PE9915x Point-of-Load Buck Regulators

Introduction

This application note provides guidelines for addressing potential output voltage overshoot which can be observed on PE9915x POL devices during fast VIN transitions, during the time VIN is below the under voltage lockout threshold (UVLO).
The intent is to demonstrate how the overshoot can be mitigated by keeping VIN slew rate at or below the rate of 100 V/s, in combination with keeping SDb low (device in shutdown mode) during the time VIN transitions, as a recommended best practice.

Product Description

The PE9915x are radiation tolerant, point-of-load (POL) buck regulators with integrated switches targeted for commercial, military, and space applications. The PE99151, PE99153 and PE99155 are designed to operate from a wide 5V bus and provide an adjustable output voltage of 1.0V to 3.6V, while delivering up to 2A, 6A or 10A of continuous current respectively. For more information, visit Teledyne e2v's power management site at https://www.e2v.com/products/semiconductors/peregrine/#tab-6

Background

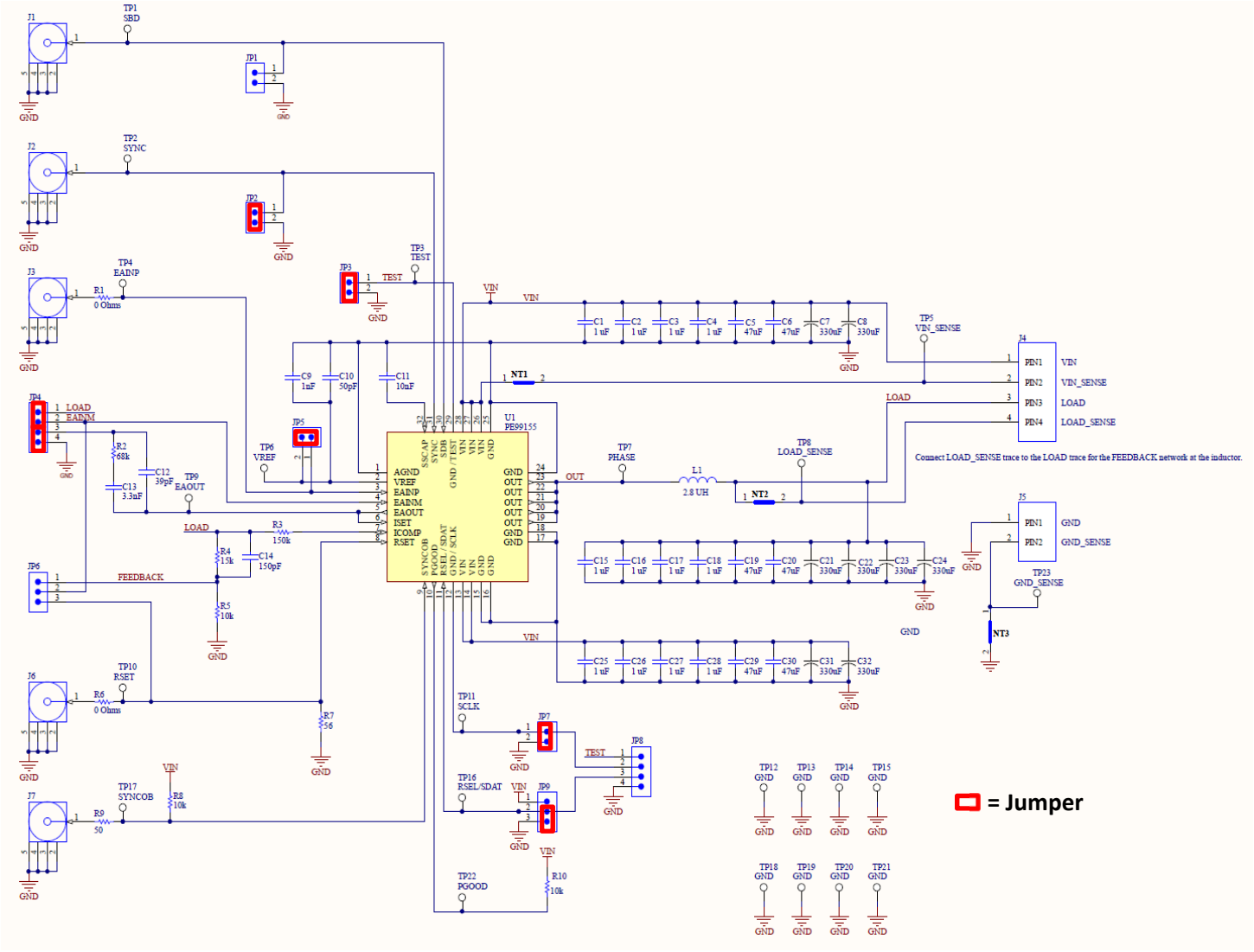
The output voltage overshoot condition is due to a design sensitivity to process variation in the level shifter used to control the gate of the high side output FET. This may cause the gate of the high side output FET to be floating when VIN is below the UVLO threshold. This floating gate condition can cause the high side output FET to turn on, when it should be in the off state during VIN transitions. Once VIN is above the UVLO threshold, output voltage regulation will return to normal operation.

It is important to note,the output overshoot can occur independent of output load and compensation component values, since when it does occur, it happens before the UVLO threshold is reached, and thus it is before the regulation control loop is even active.

Following the recommendations given in this application note will significantly reduce or eliminate the chances of the overshoot occurring in your application.

Figure 1. Bench board schematic used for taking the scope plot examples shown in this document, along with the jumper settings used.

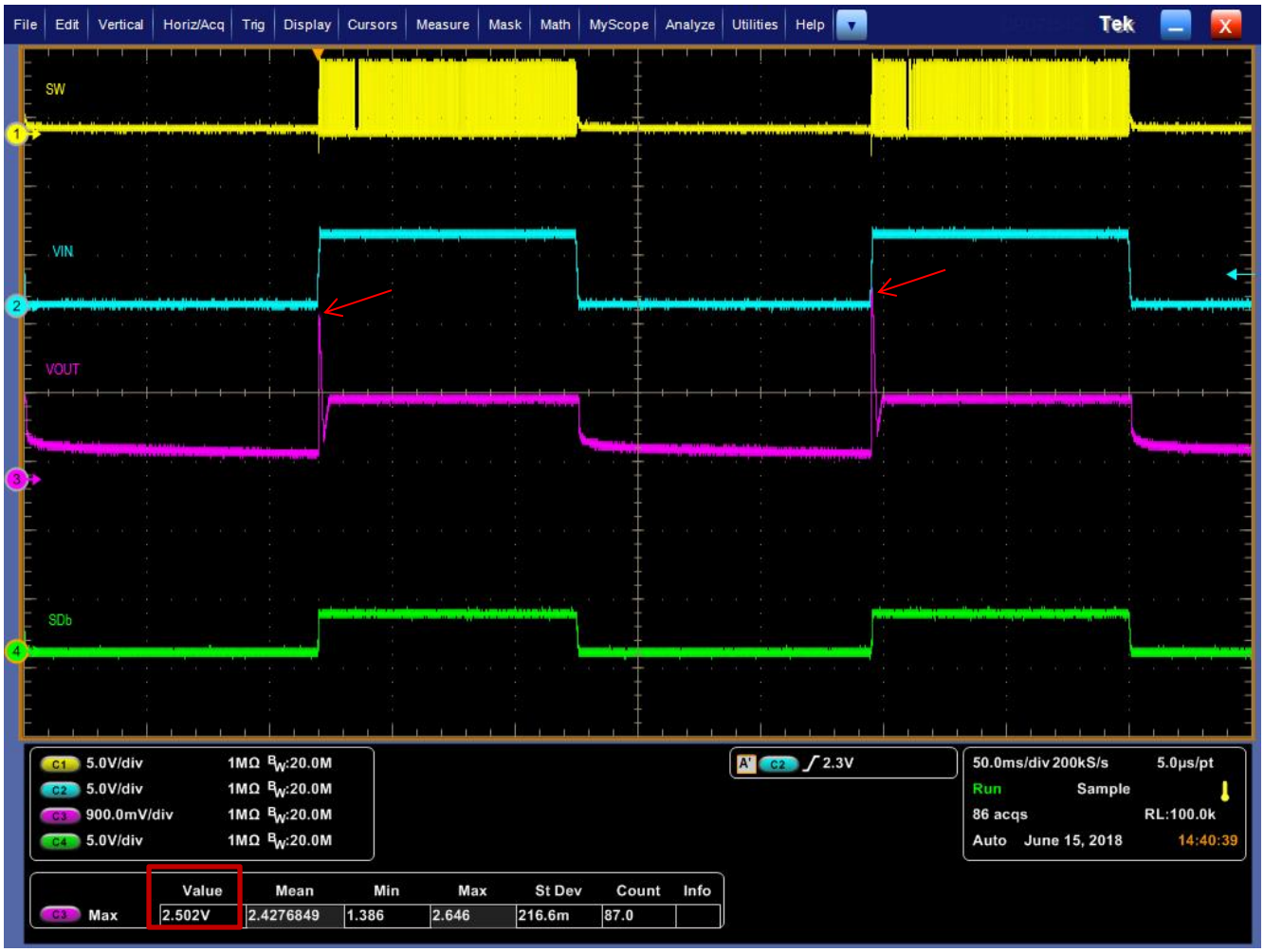
Figure 1. PE9915x Board Schematic Used for Scope Plots



Examples Cases of Output Voltage Overshoot

Figure 2. Oscilloscope plot of a PE99155 unit that is exhibiting the output voltage overshoot during the low-to-high VIN ramp. In this example, VIN is toggled between 0V and 5V, and is ON for 100ms and OFF for 100 ms, using a 10,000 V/s slew rate. The output voltage regulation set point is 1.0V. The internal current limit is being used. The output inductor is 2.8 µH, and the output capacitance is roughly 1.4 mF total. The SDb was pulled up to VIN via the internal 40 kΩ resistor. There is no load on the output, but the overshoot can happen even with full load.

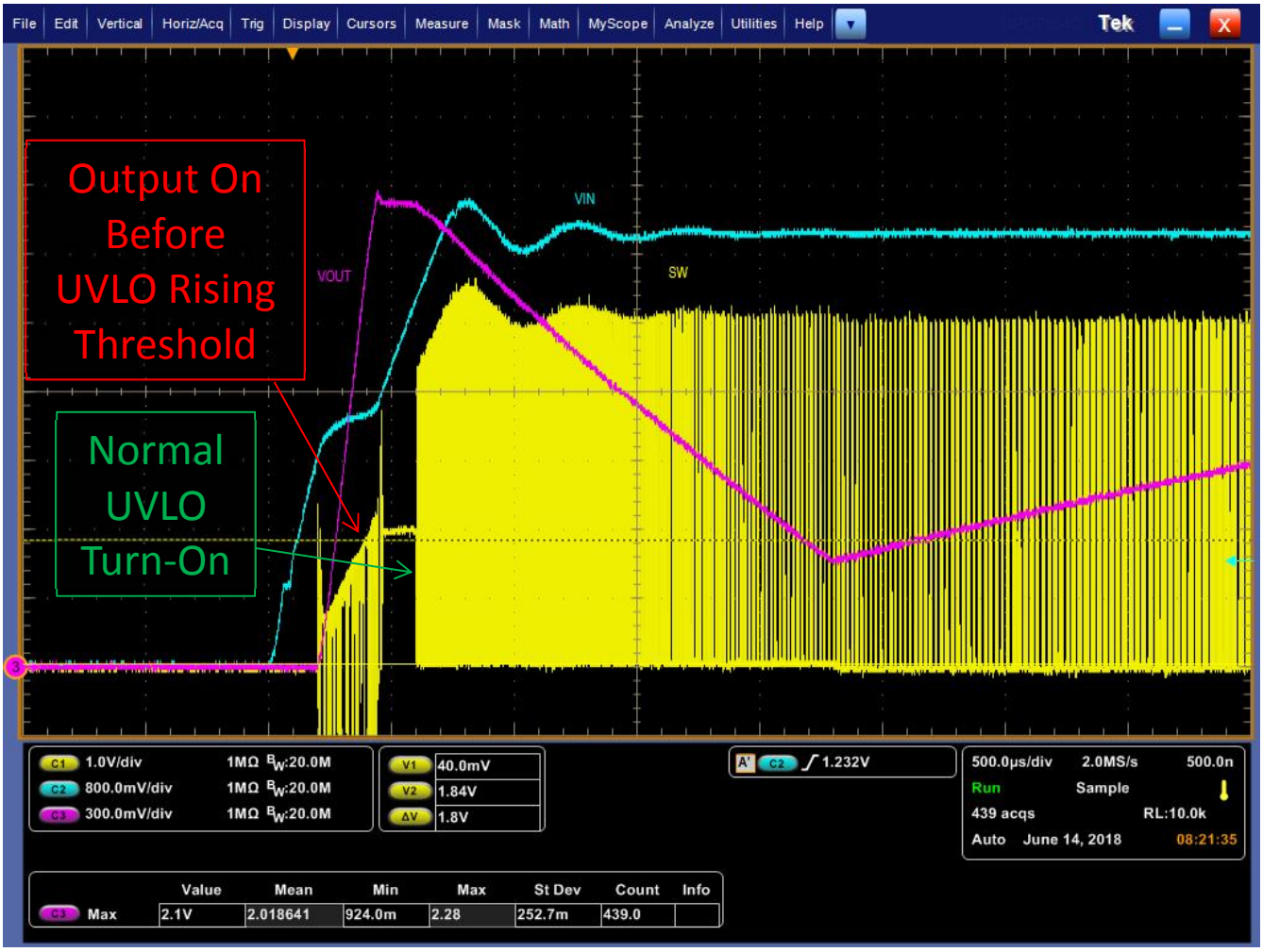
Figure 2. Plot Showing VOUT Overshoot to 2.5V with 10,000 V/s VIN Slew Rate.



CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Figure 3. Zoom-in of the voltage overshoot observed in **Figure 2.**, with a VIN slew rate of 10,000 V/s. The switch node output (SW) starts to turn on when VIN is below the UVLO threshold, then once the normal UVLO threshold is reached, the output begins switching normally and the output ultimately goes back to the 1.0V regulation set point.

Figure 3. Zoom-In Plot of VOUT Overshoot



CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Figure 4. Same device as the plot in **Figure 2**, but this time the VIN slew rate is reduced to 1,000 V/s. Note that the overshoot on the output still exists on the rising edge of VIN, but now the amplitude of the overshoot is reduced. It is, however, still exceeded the targeted set point of 1.0V

Figure 4. Plot of Same Unit, with the VIN Slew Rate Reduced to 1,000 V/s

CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Note that by reducing the VIN slew rate from 10,000 V/s to 1,000 V/s, the maximum output voltage is now only going to 1.386V, instead of 2.5V, as it did with a 10,000 V/s VIN slew rate.

Figure 5. Shows how decreasing the VIN slew rate to 500 V/s reduces the output overshoot even further, to where we now see the output voltage going to 1.13V maximum.

Figure 5. Plot of Same Unit, with VIN Slew Rate Reduced to 500 V/s

CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Figure 6. Scope plot of the same unit and same setup, but this time with the VIN slew rate reduced down to 300 V/s. With this slew rate, the output overshoot was eliminated completely.

Figure 6. Plot of Sam Unit, with VIN Slew Rate Reduced to 300 V/s.

CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Note: *For extra margin, we recommend using a VIN slew rate of 100 V/s or less, even though 300 V/s was sufficient for the units we tested.*

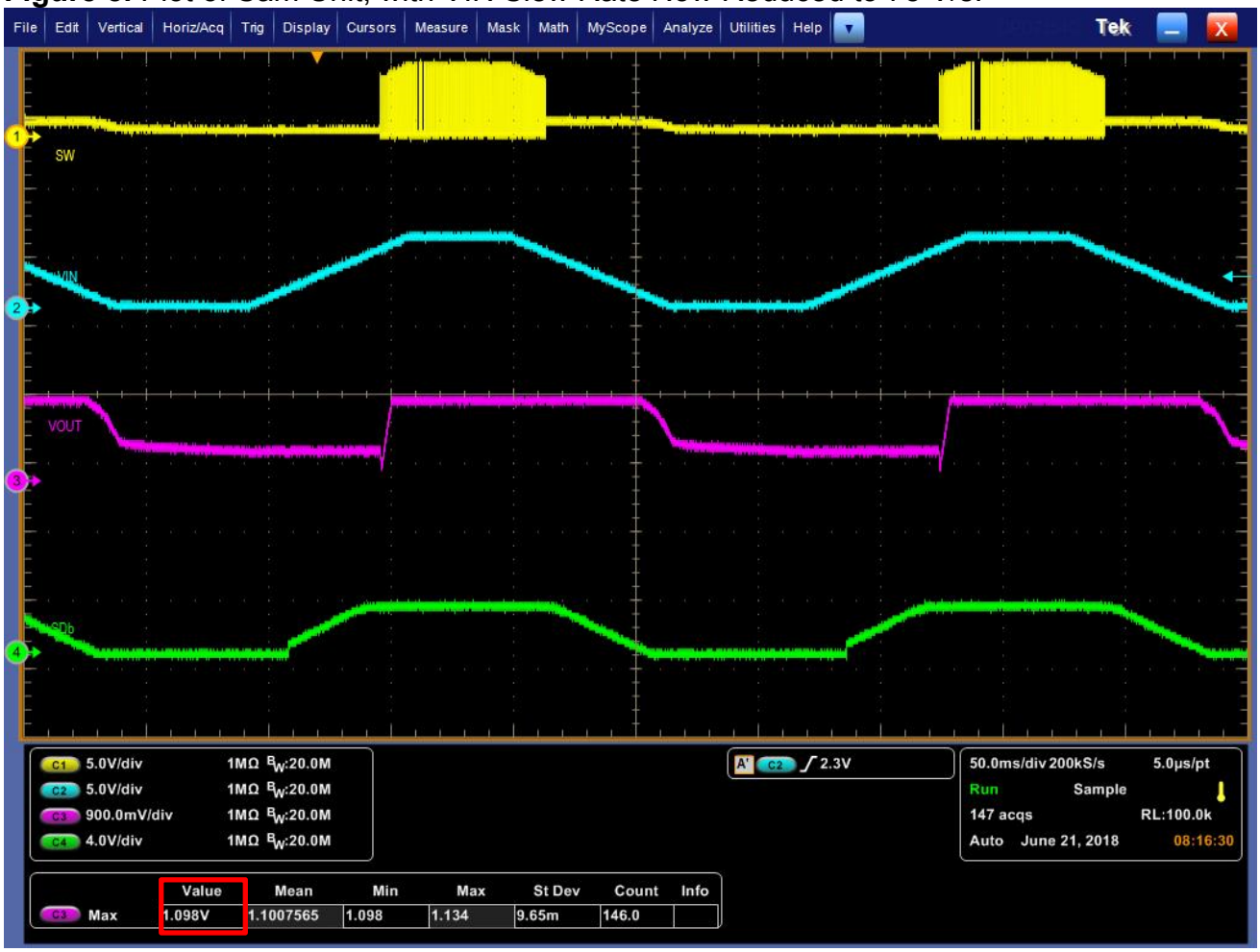
Figure 7. Scope plot of the same unit and same setup, but this time with the VIN slew rate reduced down to 100 V/s. In this case, the output overshoot is also eliminated completely.

Figure 7. Plot of Sam Unit, with VIN Slew Rate Now Reduced to 100 V/s.

CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Figure 8. Scope plot taken on the same unit with the same setup, but with the VIN slew rate reduced down to 75 V/s. This was done to illustrate that slew rates below 100 V/s also have no issue with output overshoot.

Figure 8. Plot of Sam Unit, with VIN Slew Rate Now Reduced to 75 V/s.



CH1 (Yellow): Output switch node before the output inductor at TP7 in **Figure 1.**
CH2 (Cyan): VIN Supply Voltage
CH3 (Magenta): VOUT Output Voltage at TP8 in **Figure 1.**
CH4 (Green): SDb Pin

Figure 9: Example where Toggling SDb=Low During VIN Transitions Helps on Some Units.

SDb Tied to VIN **SDb Low During VIN Transitions**

In **Figure 9**. above, the plot on the left shows the case where SDb is tied to VIN through the on-die 40 kΩ resistor. The VIN slew rate is 10,000 V/s. The output regulation set point is 1.0V, and the output is observed reaching just over 2.5V maximum. For the plot on the right, the SDb pin is pulled low with a 3.3V GPIO port, then brought high 1ms *after* VIN reaches 5.0V. It is also being commanded low just before VIN starts to transition low. In this case, even with a VIN slew rate of 10,000 V/s, the output overshoot was eliminated.

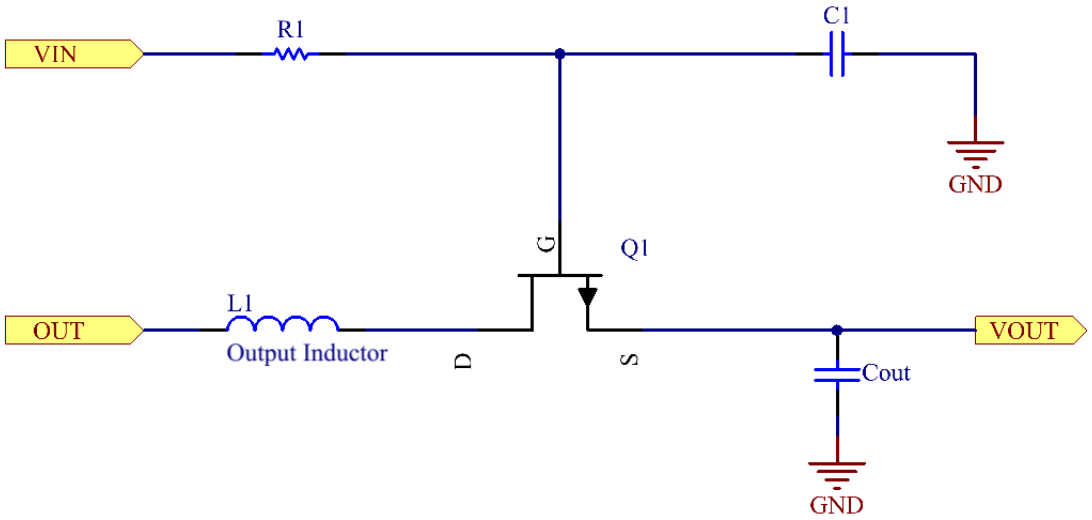
Note: *It is still recommended to reduce VIN slew rate to 100 V/s or less as well as keeping SDb low during VIN transitions, since only keeping SDb low during VIN transitions with a 10,000 V/s slew rate did not solve the startup overshoot in every case on units we tested.*

Summary

Some PE9915x POL devices may exhibit an output voltage overshoot during VIN transitions, especially on the rising edge of VIN, and especially if the VIN slew rate is faster than 100 V/s. In order to prevent or greatly reduce the chance of this happening, and keep the output voltage regulated within the specified datasheet tolerance, the following guidelines are recommended:

- Minimize VIN transitions as much as possible. The less VIN transitions you have, the lesser the chance of startup overshoot occurring.
- Keep VIN slew rates at or below 100 V/s.
- It is also recommended to keep the SDb pin pulled low during VIN transitions, and only have SDb go high after VIN Is above the VIN=4.6V minimum operating supply voltage.
- If there is still concern over the potential for output voltage overshoot, or a VIN slew rate of 100 V/s or less is not possible, then an external pass FET with an RC filter from VIN to the gate of the external FET can be used to isolate the output from the overshoot during the rising edge VIN transition. **Figure 10.** shows an example schematic. The values of R1 and C1 can be adjusted to suit the time constant and Vt of the FET used. This FET should have the following characteristics:
    - Must be able to support full load and short-circuit currents in the application.
    - Should have low Rdson to reduce losses.
    - Should be radiation tolerant for space applications.
    - GaN FETs are a possible candidate, due to radiation tolerance and typically low Rdson.

Figure 10: External FET Example to Mitigate Output Overshoot.



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