Implementing Design Features of the PE9915x Point-of-Load Buck Regulator

Introduction

This application note provides details on implementing key design features and options available on Peregrine Semiconductor's PE9915x DC-DC converters. These features include frequency (clock) synchronization, power sequencing, soft start and current sharing, which are critical factors in field-programmable gate array (FPGA) and application-specific integrated circuit (ASIC) power management design. Additional features such as adjustable loop compensation, slope compensation and over current protection are discussed in more detail in the device datasheets.

Summary

- Frequency synchronization feature enables two or more converters to be locked together to improve system performance
- Soft start option provides power control to the load by limiting the output voltage ramp rate
- Independent power good, enable and soft start pins allow simple power sequencing approaches for driving digital loads
- Current sharing feature increases total output current availability through parallel operation of two or more converters

Product Description

The PE9915x are radiation tolerant point-of-load (POL) buck regulators with integrated switches targeted for commercial, military and space applications. The PE99151, PE99153 and PE99155 are designed to operate from a wide 5V bus and provide an adjustable output voltage of 1.0V to 3.6V while delivering up to 2A, 6A or 10A of continuous current respectively. For more information, visit Peregrine's power management site at www.psemi.com.

Frequency Synchronization

The noise generated by switching power supplies can disturb sensitive circuitry when the switching frequency is not synchronized to the system's clock frequency. Synchronization enables two or more regulators to be locked together to one frequency and can also be used to eliminate beat frequencies generated by the interaction of multiple DC-DC converters.

The PE9915x contains an internal oscillator capable of operating at 1 MHz when the SYNC pin is tied to V_{IN} (or left open) or at 500 kHz when the SYNC pin is tied to ground. This reference clock is used in the current mode control loop to time the rising edge of the OUT pin and as a global internal clock reference. Alternatively, the SYNC pin may be externally clocked at a rate of 100 kHz to 5 MHz. In this case, the internal oscillator uses the clocked sync pulse train as the global internal clock reference. If the synchronization clock is removed or not present during startup, the internal oscillator will default to 1 MHz or 500 kHz depending on the state of the SYNC pin.

The SYNC feature offers design flexibility because the switching frequency determines critical system parameters including component size, efficiency, noise, loop bandwidth and circuit board area. A higher switching frequency allows the use of smaller inductance and output capacitance to obtain a lower ripple voltage, wider loop bandwidth and faster transient response. A lower switching frequency may be preferred for higher efficiency. The SYNC frequency may also be selected to control switching noise generated by the converter in order to prevent electromagnetic immunity (EMI) and spurious interference.

An inverted clock signal is provided by the SYNCOb pin of the PE9915x converter. Driving additional converters 180 degrees out-of-phase can reduce the amplitude of input currents, the physical size and the electrical requirements of the input capacitance.

Soft Start

Soft start may be implemented to allow the PE9915x to slowly ramp to its steady state operating voltage. This feature has the advantage of limiting the output voltage rise time to prevent overshoot. The output voltage rise time can be increased by tying the SScap pin to the 5V input rail through an external resistor. The ramp rate can be decreased by connecting the SScap pin to ground through an external capacitor (Css). An initial current is set by an internal regulator, VLDO (3.2V) and an internal pull-up resistor R (1.2 mΩ) to charge Css. The desired soft start time can be calculated from

*SS time (seconds) = –R*Css*ln [1 – (VREF/VLDO)],*

where VREF is the internal reference voltage of 1V.

Many FPGA datasheets have specific power supply ramp time requirements that can be implemented with a soft start capacitor. *Table 1* shows a list of soft start capacitor values and the resulting soft start times.

Table 1. Soft Start Capacitor Values with Associated Soft Start Times

Css (nF)	Soft Start Time (ms)
No cap	0.45
10	4.5
22	10
39	18
100	45

Power Sequencing

Some FPGAs, digital signal processors (DSPs) and other microprocessors may require sequencing and/or tracking between supply voltages to avoid latch-up or damage. When multiple PE9915x regulators are used in a distributed system, a sequential start-up routine can be implemented using the power good, shutdown (SDb) and soft start features. This involves connecting the PGOOD pin of one converter to the SDb pin of the following converter as shown in *Figure 1*. In this case, when the first converter (PE99155-10A) reaches 90% (typ.) of its final output value, its PGOOD pin will supply a signal to the SDb pin of the second converter (PE99153-6A) allowing it power up. Likewise, when the second converter reaches 90% (typ.) of its final output value, its PGOOD pin will supply a signal to the SDb pin of the third converter (PE99151-2A) allowing it power up. The sequential start-up waveform response in *Figure 3* shows how the core voltage is powered up first, followed by the auxiliary and then the I/O voltage.

The soft start feature can also be combined in a distributed system using power sequencing to control the rise time of the output waveforms using a simultaneous start up scheme. This approach uses a common enable control to simultaneously activate each converter and requires manipulation of the soft start capacitor to position each slew rate as shown in *Figure 2*. The resulting start up waveform response is shown in *Figure 4*.

If all output voltages need to be at the final regulated voltage at the same time, a ratio-metric approach may be used. This technique uses the same configuration as the simultaneous start up approach in *Figure 2* with the exception that all soft start capacitors have the same value. A 10 nF soft start capacitor was used on each converter for the resulting startup waveform response shown in *Figure 5*.

Current Sharing

When higher output currents are required, two or more PE9915x converters rated at the same maximum output current and operating at the same frequency may be connected in a parallel configuration to enable a technique known as current sharing. The resulting load current capability will be the sum of the total currents of each regulator.

Proper current sharing requires that each converter deliver an equal amount of current to the load. Since the output impedance of switching regulators is very low, small differences in the output voltages between the parallel converters will result in an imbalance of current between them. If the design does not allow for currents to be equal, some converters may conduct more than others resulting in unequal sharing.

The PE9915x DC-DC converters incorporate robust traditional peak current mode control architecture for power management solutions under extreme conditions. Current mode control is the ideal architecture for current sharing because it maintains direct control of the switch current through a common control voltage. The key to effective current sharing between two or more PE9915x converters is the current accuracy provided by the ISET pin. The current mode control threshold current is set by the ISET pin, which is driven by the voltage control loop from the output of the error amplifier. The PE9915x takes the voltage applied to the ISET pin, subtracts 0.7V (typ.) and applies that voltage to the RSET resistor. The current flowing through the RSET resistor is then used as a scaled current reference for the inductor current threshold comparison. Operating two or more devices in parallel using this scaling factor as a reference insures the currents are equally shared.

Current sharing is implemented with the PE9915x by connecting the RSET pin of the master converter to the EAINP pin of the slave converters and the EAINM to the RSET of each slave converter as shown in *Figure 6*. It is recommended to keep the connections short using low impedance paths to reduce noise pickup. Frequency synchronization is achieved by connecting the SYNCOb pin of the master converter to the SYNC pin of the slave converter through a pull-up resistor. Operating each device at a common frequency using a synchronous clock eliminates the beat frequency that can be present between the converters.

Figure 7 shows the resulting current sharing equality between two 10 amp PE99155 POL buck regulators. *Figure 8* shows the shared output voltage ripple, *Figure 9* shows the shared efficiency, and *Figure 10* shows the resulting load transient response for a 0 to 14A load current step.

Figure 1. Sequential Power Sequencing Distribution Using Enable and PGOOD Features

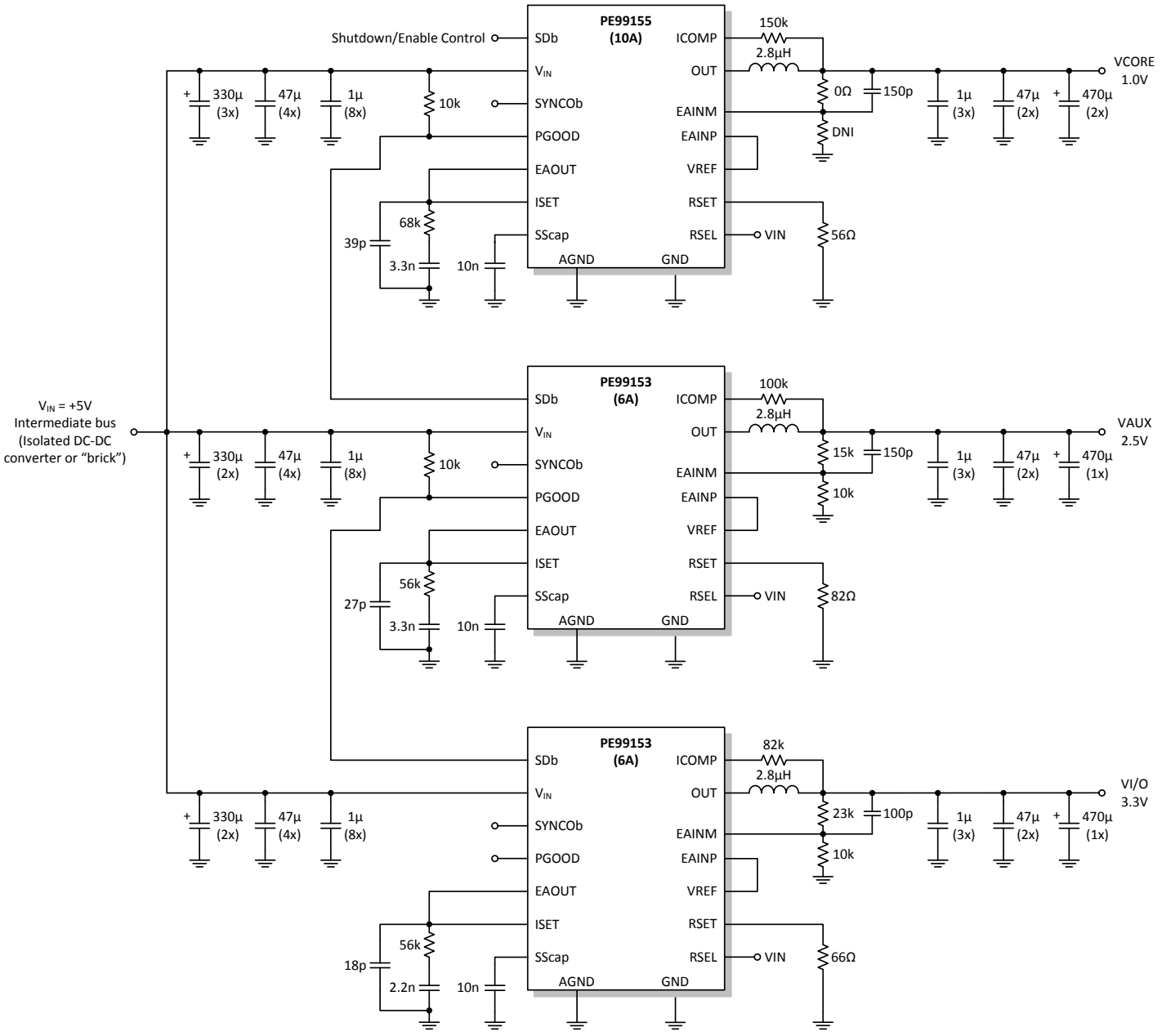


Figure 2. Simultaneous Power Sequencing Distribution Using Common Enable Control and Soft Start Features

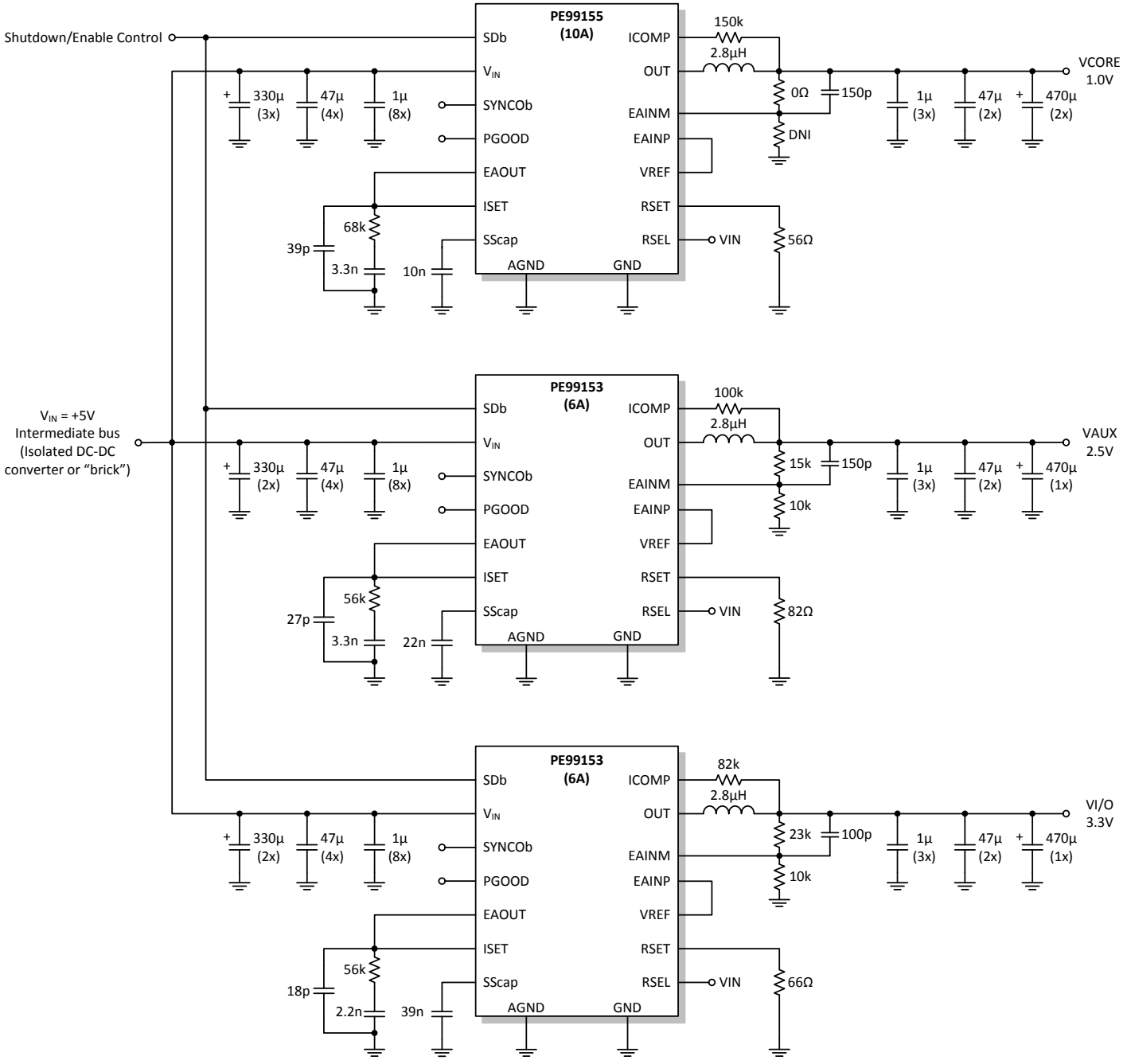


Figure 3. Sequential Power Sequencing Waveforms Using Enable and PGOOD Features

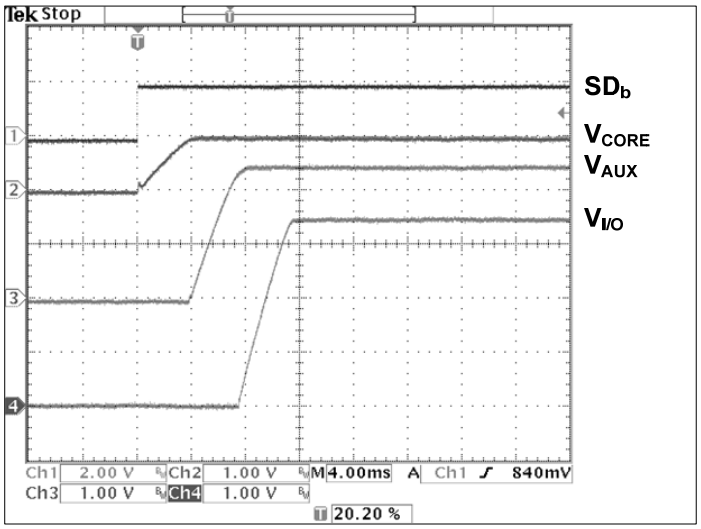


Figure 4. Simultaneous Power Sequencing Waveforms Using Common Enable Control and Soft Start Features

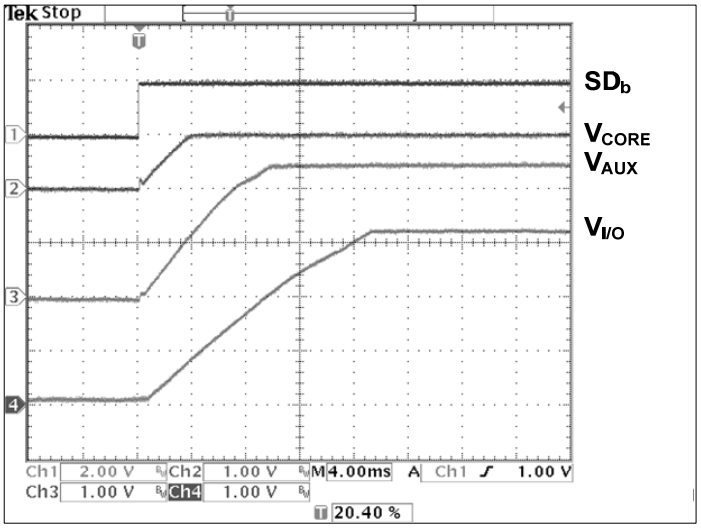


Figure 5. Ratio-metric Power Sequencing Waveforms Using Common Enable Control

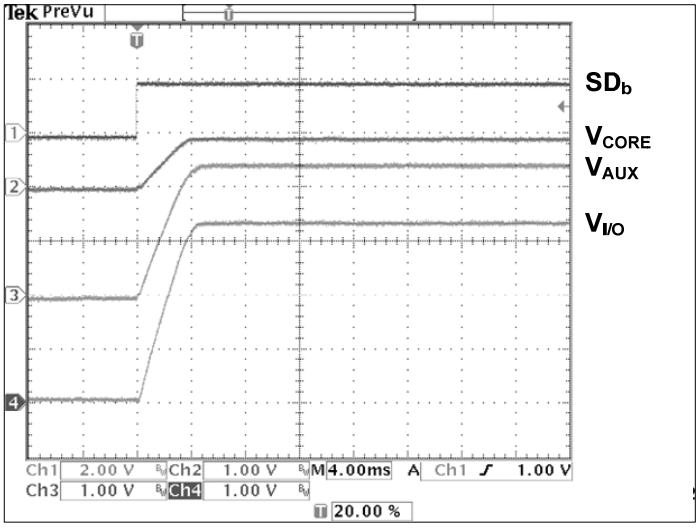


Figure 6. Current Sharing and Synchronization Configuration Using Two PE99155 Buck Regulators

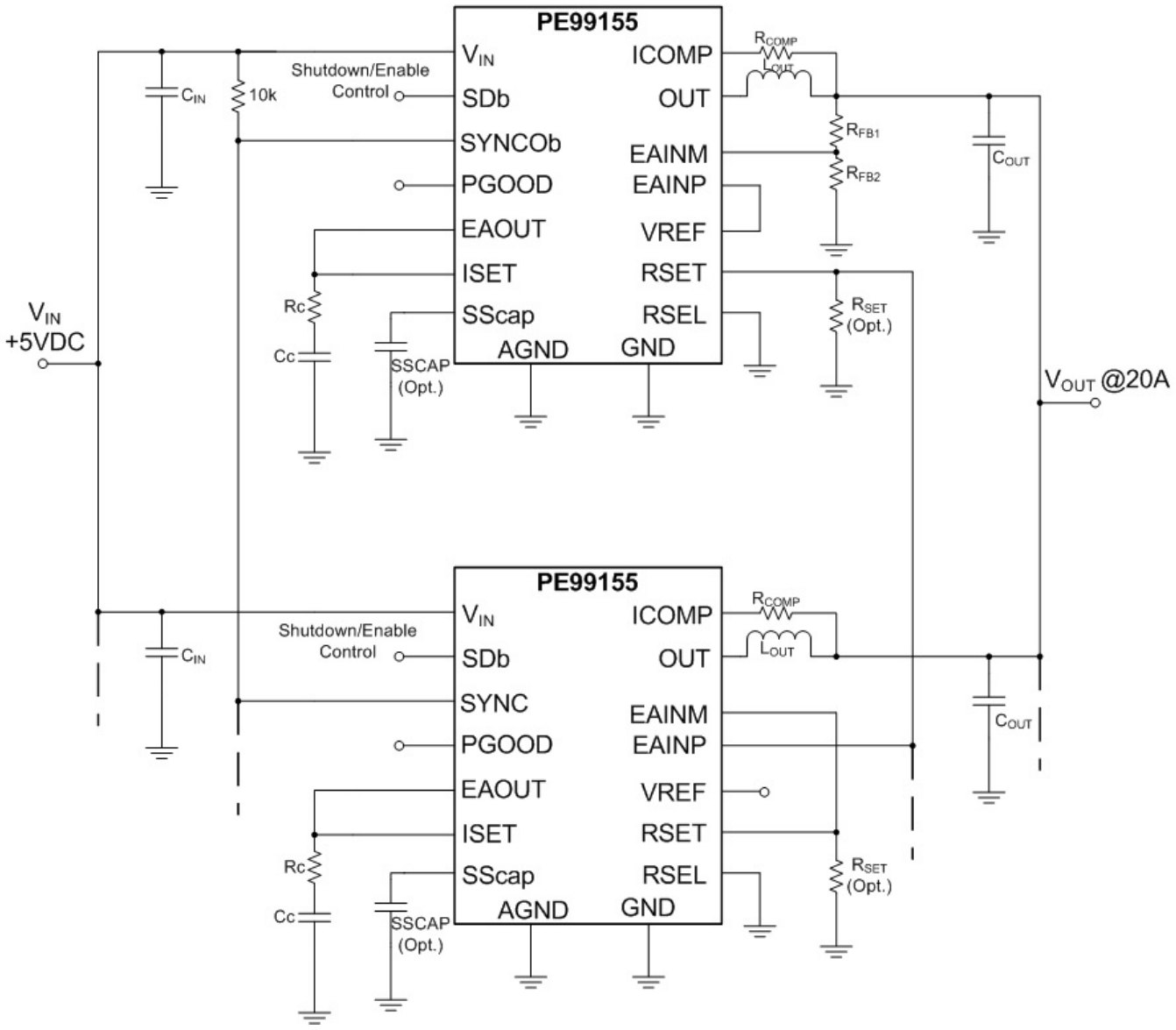


Figure 7. Current Sharing Accuracy

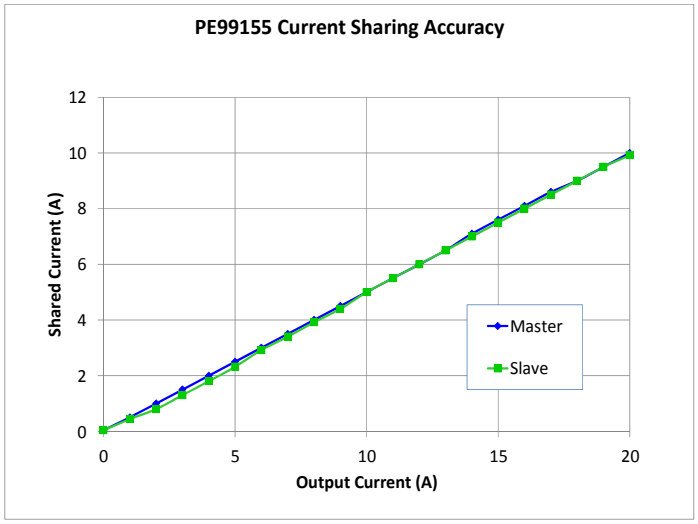


Figure 8. Output Voltage Ripple for Current Sharing Configuration (V_{IN} = 5V, V_{OUT} = 1.0V, F_{SW} = 500 kHz)

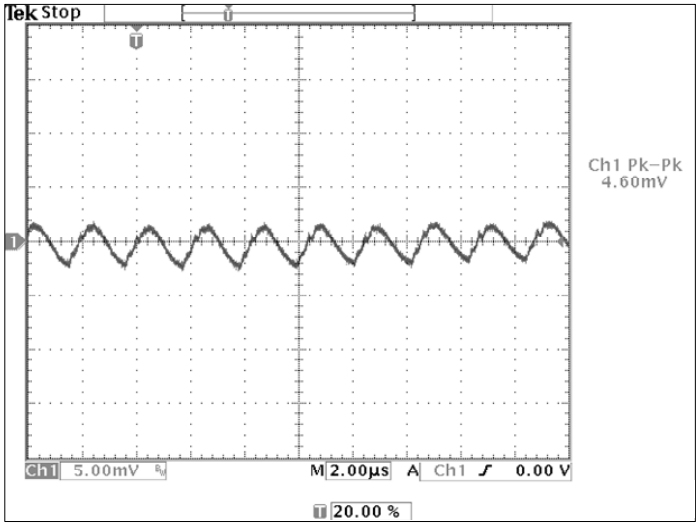


Figure 9. Current Sharing Efficiency

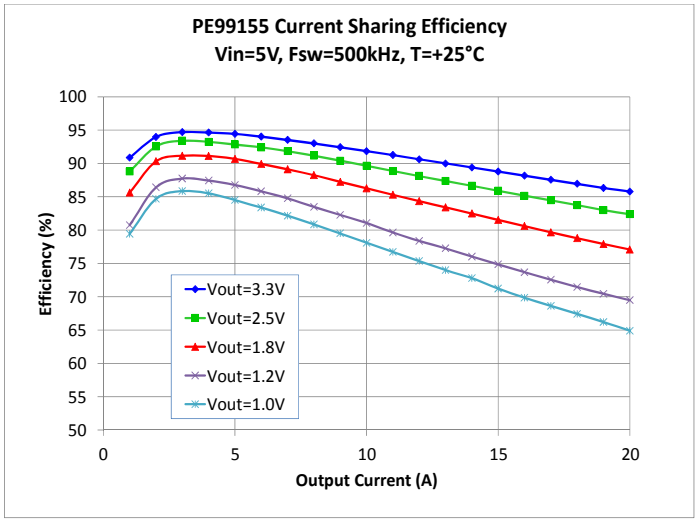
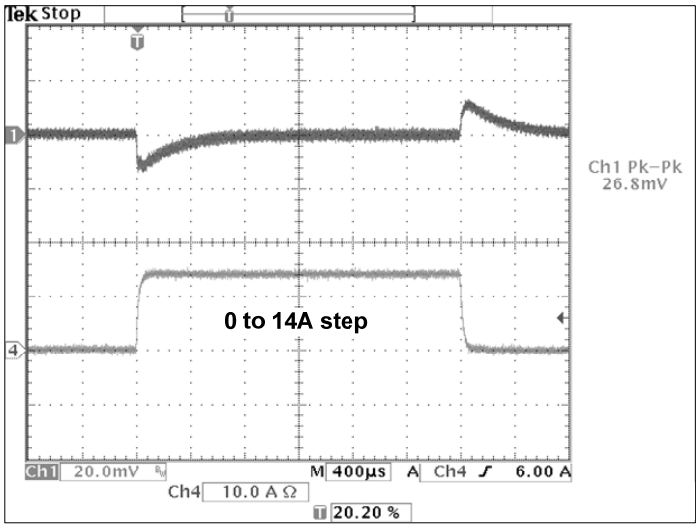


Figure 10. Current Sharing Load Transient Response for a 0 to 14A Current Step (V_{IN} = 5V, V_{OUT} = 1.0V, F_{SW} = 500 kHz)



Conclusion

The PE9915x highly integrated POL buck regulators offer a full range of features and options enabling the designer to meet their power management needs. Frequency synchronization improves system performance by allowing multiple converters to share the same frequency. Soft start can be used to control the output voltage rise time. Several power sequencing options are easily configurable based on design requirements. Accurate current sharing can be simply implemented to increase the maximum output current if required.

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