Radiation Tolerant Power Management Solution for Xilinx Virtex-5 Space-Grade FPGAs

Introduction

Highly reliable, space-qualified distributed power systems are necessary to meet the power requirements of high-performance, space-grade signal processing devices. Complex start-up conditions coupled with transient behavior and sequencing requirements make power management an important factor in field-programmable gate array (FPGA) system design. Radiation tolerant point-of-load (POL) DC-DC converters operating at low output voltages and capable of delivering high currents can meet these stringent demands.

This application note presents power management solutions for the Xilinx radiation tolerant, space-grade Virtex-5QV FPGA using Peregrine Semiconductor's high-reliability (Hi-Rel) POL buck regulator products. A distributed power system using two or more POLs will be presented.

UltraCMOS® Technology

Peregrine Semiconductor's Hi-Rel products are specifically designed for space and satellite applications. UltraCMOS proprietary CMOS-on-sapphire technology makes this possible. The insulating substrate eliminates the parasitic 4-layer device structures present in bulk silicon, making radiation-induced latch-up impossible. Drain capacitance is also virtually eliminated and since the parasitic drain capacitance does not need to be charged and discharged on every cycle, dramatic improvement in transistor performance is realized.

Summary

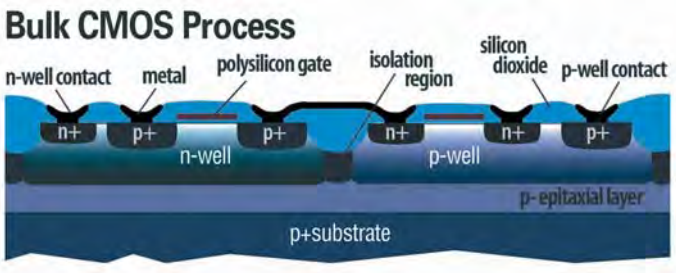
- Xilinx Virtex-5QV space-grade FPGA requires low supply voltages and high operating currents from multiple power rails
- PE9915x radiation tolerant POL buck regulators offer power management solutions for the Virtex-5QV
- Peregrine's UltraCMOS® technology improves transistor performance and provides immunity to radiation-induced latch-up
- Presented distributed power solution offers huge advantages in reliability, size, weight and cost

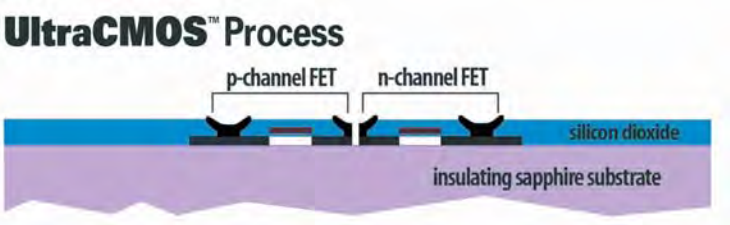
The insulating substrate also provides better isolation between circuit elements, improved thermal conductivity and FET stacking capability for higher voltage handling.

PE9915X Radiation Tolerant POL Buck Regulators

The PE9915x monolithic, POL synchronous buck regulators with integrated switches are designed to operate from a wide 4.6V to 6V bus (5V ±10% recommended) and provide an output voltage of 1.0V to 3.6V while delivering up to 2A, 6A or 10A of continuous current. These parts deliver excellent peak power efficiency (>93%) while high substrate thermal conductivity minimizes thermal concerns. The internal oscillator can operate at 500 kHz or 1 MHz.

Figure 1. UltraCMOS vs Bulk CMOS Process





Optionally, the switching frequency can be synchronized to an external reference from 100 kHz to 5 MHz. Current limiting is adjustable with an external resistor and is achieved through peak current mode control. An external resistor also provides adjustable slope compensation to optimize stability and closed loop bandwidth across output voltage and switching frequency range. Loop compensation is externally adjustable to meet application transient response while still maintaining stability requirements. The output is tri-stated when the shutdown/enable (SDb) pin is low to enable hot-spare capability. All products are latc-up immune (SEL), total dose tolerant to >100 kRad and highly resistant to single event effects (SEE)/single event upset (SEU) effects.

Table 1. PE9915x Radiation Test Results

TID	100 kRad(Si)
SEL	> 90 MeV•cm^2/mg
SEB	> 90 MeV•cm^2/mg
SET	> 90 MeV•cm^2/mg
SEFI	> 90 MeV•cm^2/mg
SEGR	> 90 MeV•cm2/mg

SEL, SEB, SEGR, SEU, SEFI: None observed, Au/60 degrees.
SET: No events exceeding 30 mV transient observed @ Au, LET=90, 60 degrees and normal incidence.
The UltraCMOS process does not exhibit enhanced low-dose-rate sensitivity (ELDRS) since bipolar minority carrier elements are not used.

Xilinx Virtex-5QV Power Management

The Xilinx Virtex-5QV is a single event immune re-configurable FPGA designed to meet the high-performance requirements of space applications. The Xilinx Virtex-5QV requires multiple power rails including the FPGA core, the I/O, as well as additional rails for powering clocks, PLLs, transceivers, and auxiliary circuits. The required core voltage (VCCINT) is 1.0V ± 5% and can have current demands up to tens of amps depending on the number of gates being used and the clock frequency. The auxiliary voltage (VCCAUX) requirement is 2.5V ± 5%. The I/O rail can also have significant power requirements depending on the number of I/O registers used in the FPGA design.

Distributed Power Architecture

The traditional single centralized power converter or brick, which supplies the entire electrical system, exhibits large distribution power losses and low efficiency. Large bulky cables and connectors are used to overcome demands of high bus currents. The resulting system is susceptible to poor regulation and crosstalk.

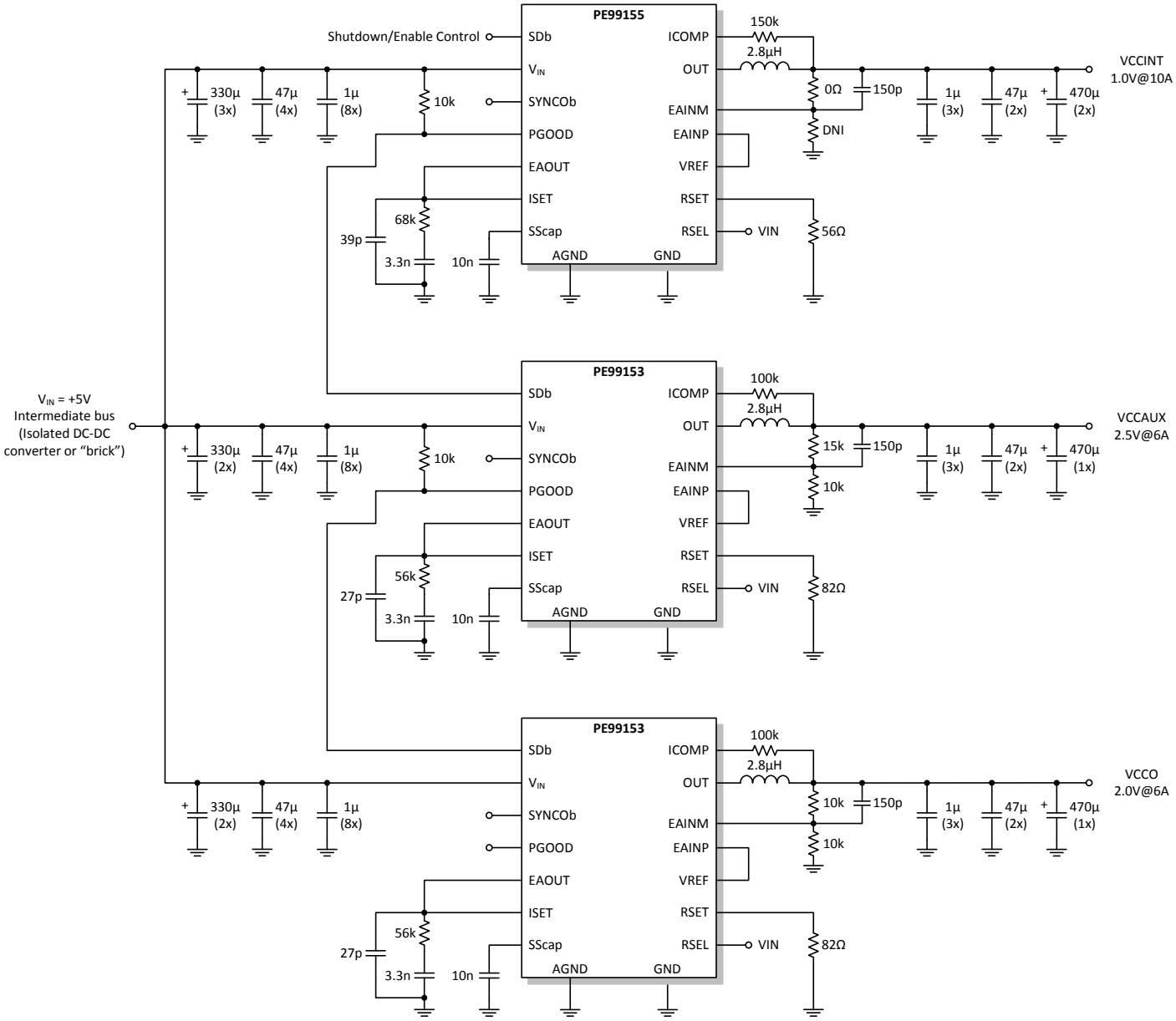
Distributed power architecture uses the intermediate bus to supply several POL s which can deliver their loads locally. This system reduces distribution losses through smaller cables and connectors, which reduce size, weight and cost. Steady state and dynamic (transient) load regulation is improved and crosstalk is reduced.

Distributed power management is a key benefit of Peregrine's POL buck regulators. *Figure 2* shows how this system may be implemented. A single PE99155 is used to supply up to 10A to the demanding FPGA core. If more power is required, a current sharing technique can be used as described in the *Current Sharing* and *Synchronization* sections. The lower current PE99153 devices may be used for the less demanding auxiliary and I/O supplies where load transient and output voltage ripple are still important.

Sequencing

The Xilinx Virtex-5QV FPGA does not require sequencing of its power rails, though the power-on sequence of VCCINT, VCCAUX, and VCCO is common. Sequentially ramping up power rails one after another will minimize in-rush current at startup and can eliminate FPGA lock-up or damage. Sequencing can be simply implemented by connecting the power good (PGOOD) pin of the core or master supply to the SDb pins of the AUX and the PGOOD of the AUX supply to the SDb pin of the I/O supply, as shown in *Figure 2*.

Figure 2. Distributed Power Management Example for Virtex-5QV FPGA



Soft Start

Soft start may be implemented to limit the output voltage ramp rate. The power supply ramp time requirements for the Xilinx Virtex-5QV FPGA rails are 0.20–50 ms. The ramp rate of the PE9915x can be increased by tying the SScap pin to the 5V input rail through an external resistor. The ramp rate can also be slowed by connecting the SScap pin to ground through a supplemental capacitor as indicated in *Figures 3-5*.

Figure 3. Soft Start with No External Capacitor ~0.45 ms Risetime

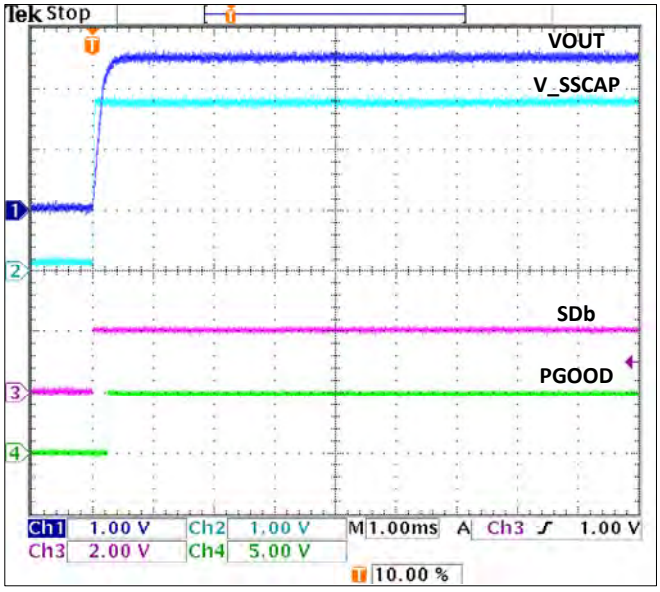


Figure 4. Soft Start with 10 nF External Capacitor ~4.5 ms Risetime

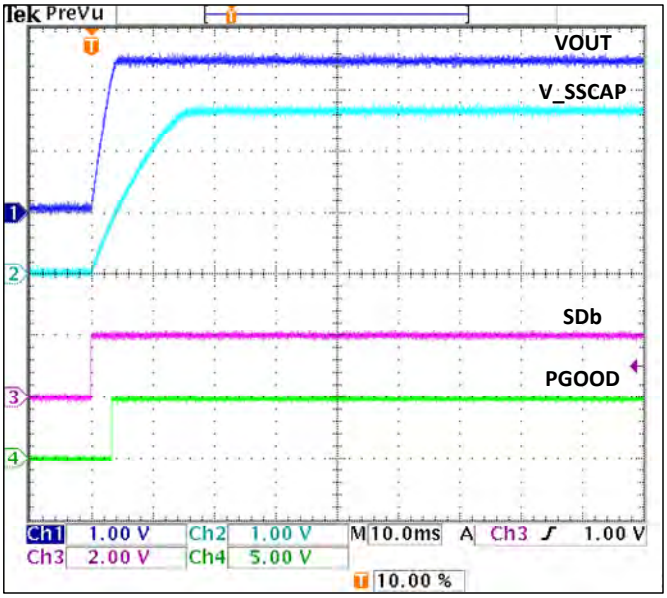
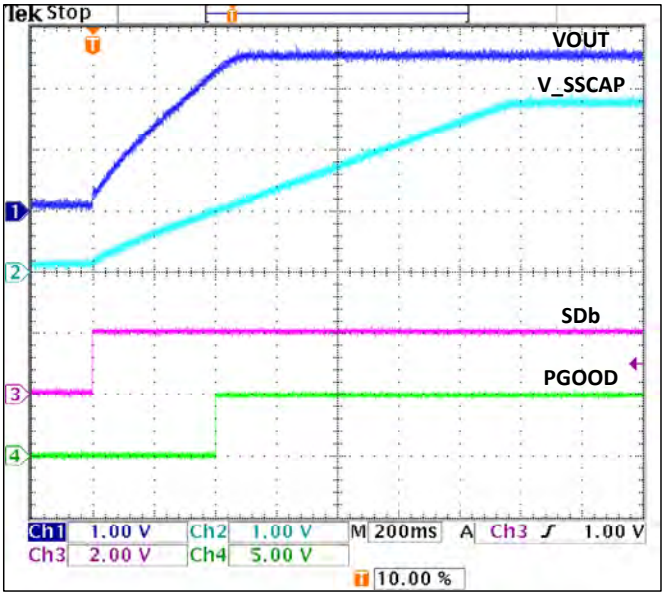


Figure 5. Soft Start with 1000 nF External Capacitor ~450 ms Risetime



Current Sharing and Synchronization

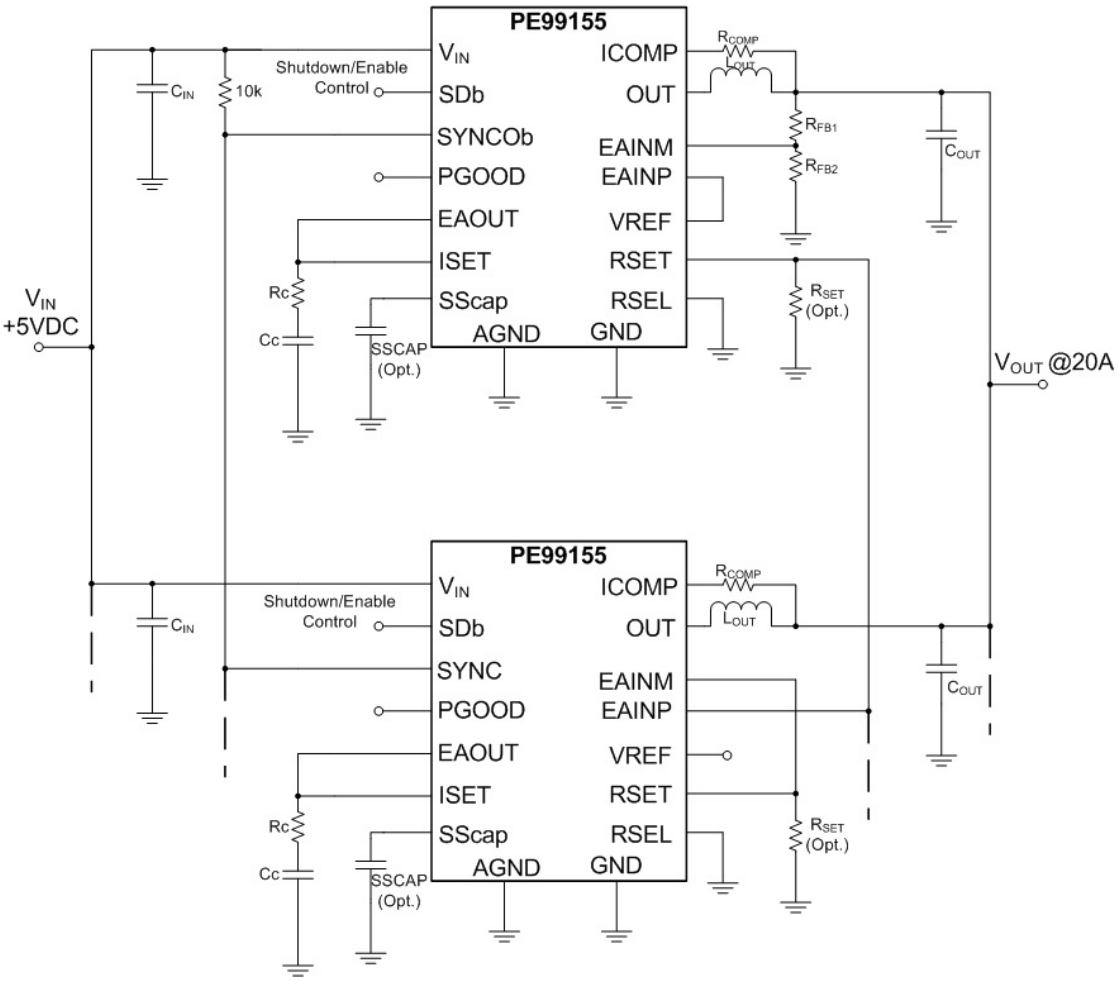
If more output current capability is required, two or more current mode regulators operating at the same frequency may be connected in a parallel configuration as illustrated in *Figure 6*. The resulting load current capability will be the sum of the total currents of each regulator.

The PE9915x contains an internal oscillator capable of operating at 1 MHz when the SYNC pin is tied to V_{IN} or at 500 kHz when the SYNC pin is tied to ground. Optionally, the switching frequency can be synchronized to an external reference from 100 kHz to 5 MHz for design flexibility. Changing the switching frequency can be beneficial in preventing spurious interference and controlling spectral emissions.

Operating each regulator at a common frequency eliminates any beat frequency interference that could result in the absence of synchronization.

Whether operating synchronously or asynchronously, the open drain SYNCOb pin contains the inverted internal clock reference. This inverted clock signal can be used to drive additional regulators. The out-of phase clock signal has the added benefit of reducing the RMS input ripple current and filtering requirements through peak current phase interleaving.

Figure 6. Current Sharing and Synchronization Example Using Two PE99155 DC-DC Converters

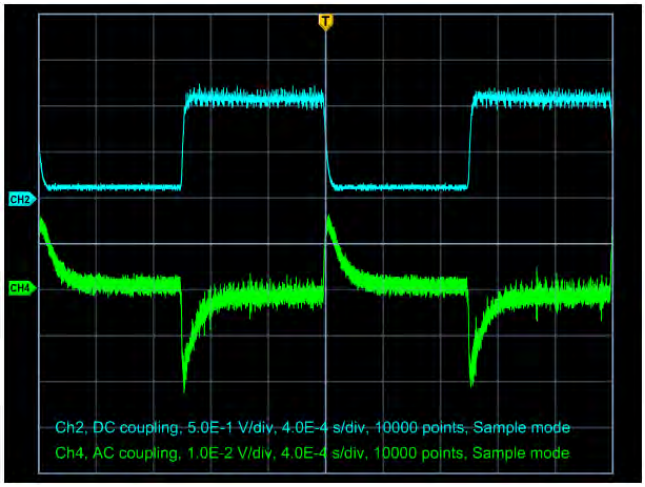


Transient Response

The core voltage of the FPGA can produce large current transients when processor loading suddenly changes from a static to a dynamic state. Under these conditions the output voltage will decrease (droop) as the load current increases and vice-versa. The power supply must be capable of delivering a large step load current while maintaining output voltage regulation in order to avoid FPGA lockup. The measure of how fast the regulator returns to steady-state conditions after a load change is known as the load transient response. The ability of the regulator to respond to a load transient is a function of the operating bandwidth in conjunction with the output capacitance. Sufficient bulk capacitance will help to absorb or source sudden changes in load current.

The PE9915x uses peak current mode control architecture, which offers excellent line regulation, simple compensation design, improved transient response and inherent cycle-by-cycle current limiting. The high switching frequency increases loop bandwidth to improve transient response and prevents interference with signal-processing circuits. An external resistor provides adjustable slope compensation to optimize stability and closed loop bandwidth across output voltage and switching frequency range. In addition, externally adjustable loop compensation allows the designer to meet transient response applications while still maintaining stability requirements.

Figure 7. PE99155 Load Transient Response, 0 to 9A transition



Noise

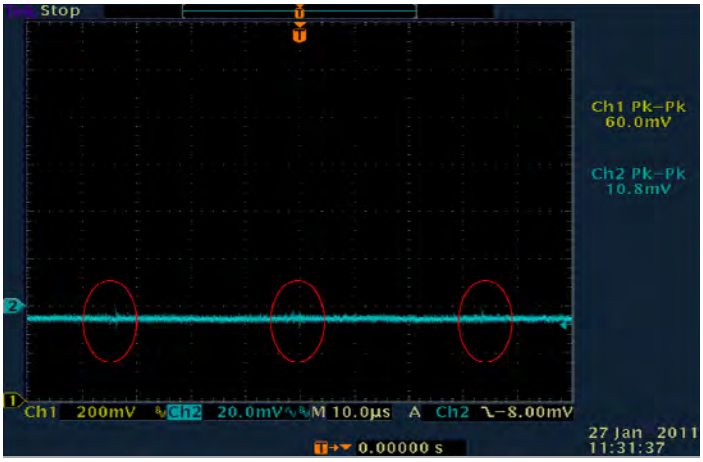
Switching converters produce a lot of baseband, harmonic and impulse noise due to the nature of operation. Good layout practices and decoupling component placement and selection can minimize output noise and conducted emissions from the input.

The maximum amount of noise present on the power supply is commonly referred to as ripple voltage. Baseband voltage ripple is minimized by bulk capacitance (low-ESR tantalum and large ceramics). To shunt inductor-winding, capacitance-coupled switching spikes at the edges, parallel lower value high-Q ceramic capacitors placed close-in to the inductor output and ground plane are important.

The input supply chops from output-load to zero current every cycle. Input capacitor equivalent series resistance (ESR) is a key term in assembly overall efficiency and to conducted emissions. AC-shorting the input current loop close-in to the IC minimizes the energy that escapes out the supply/ground lines.

The oscilloscope photos in *Figures 8-14* were taken from a standard customer evaluation board with 660 µF input and 2000 µF output filter tantalums added to the minimal bill of materials. The loop compensation network consists of a shunt 3.3 kΩ resistor/4.7 nF capacitor combination.

Figure 8. Unpowered Board (Baseline Noise)



Some ambient EMI dominates P-P readings. Note that the ambient EMI (red circles) exceeds the "real" output ripple by more than 2X.

Figure 9. PE99155 No Load Noise

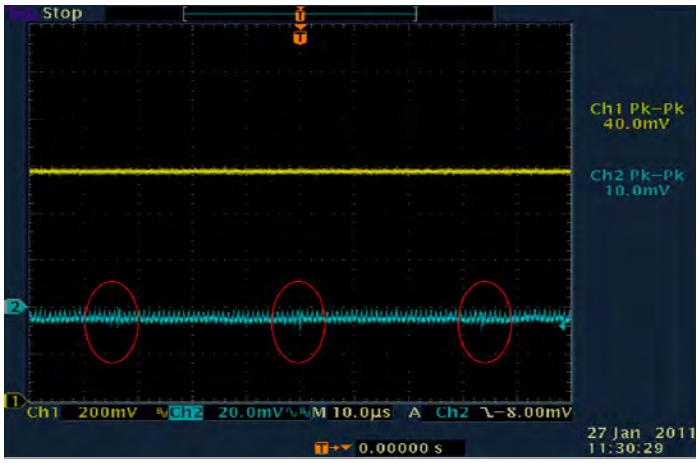


Figure 10. PE99155 Noise with 6A Load

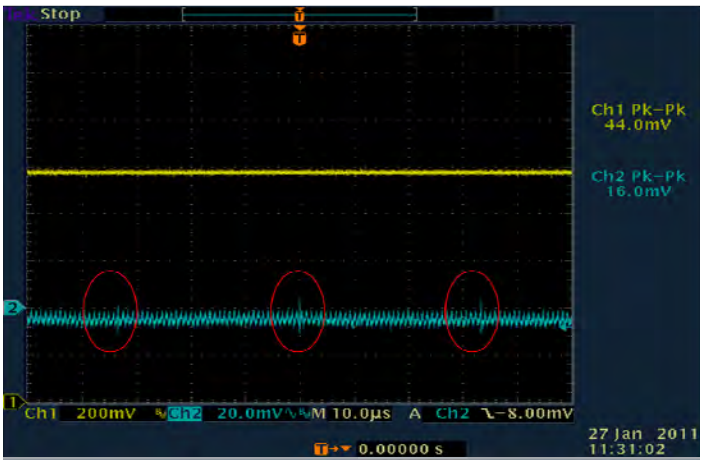


Figure 11. PE99155 Noise with No Load, Single Cycle Detail

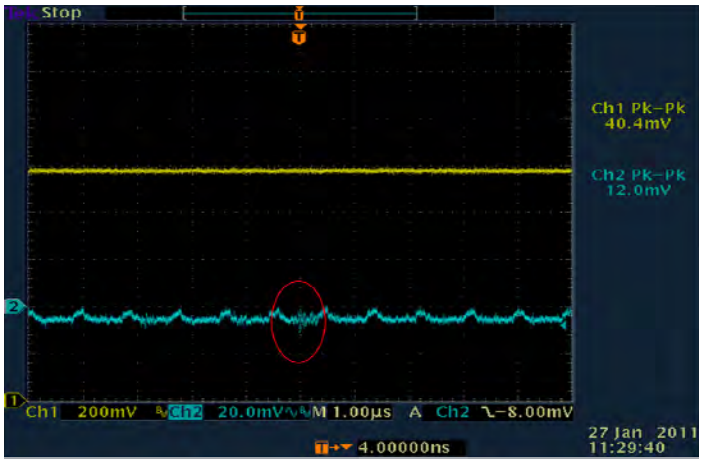


Figure 12. PE99155 Noise with 6A Load, Single Cycle Detail

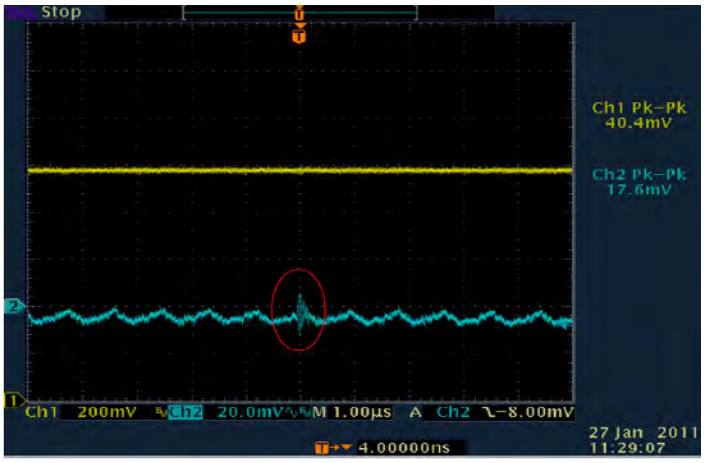


Figure 13. PE99155 Long Timescale Noise with No Load

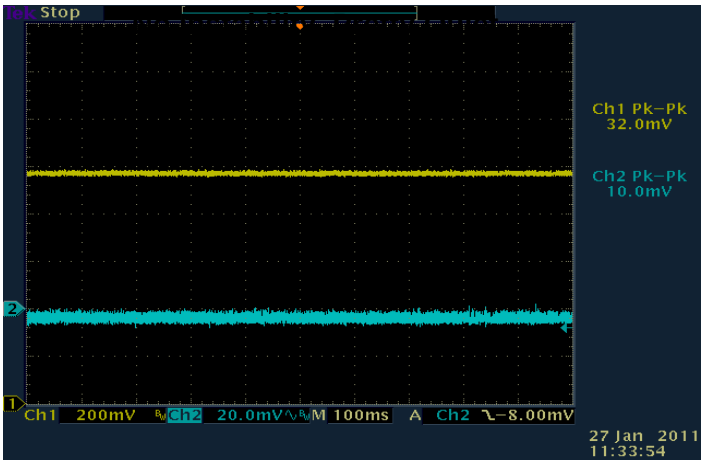
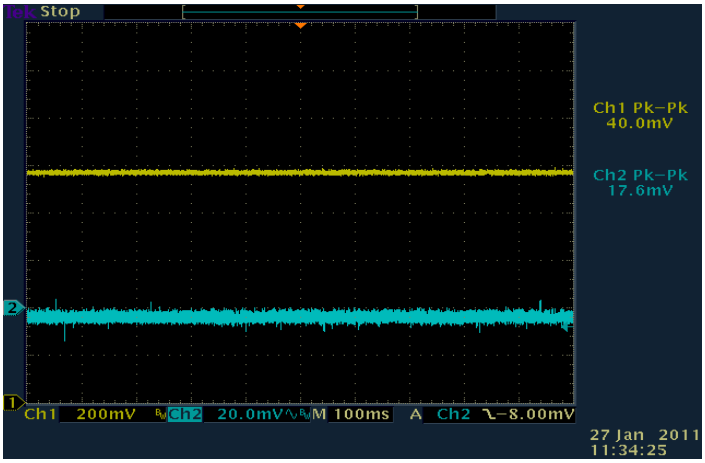


Figure 14. PE99155 Long Timescale Noise with 6A Load



Design Example

For the purposes of this application note, the Xilinx ML510 off-the-shelf commercial reference design board was used. The FPGA was programmed to step from a static operating current of 1.5A to a dynamic load current of 14A on VCCINT. *Figure 15* shows the circuit used to power the core of the Xilinx ML510 reference design board. Two PE99155 POLs operating at 1 MHz were used in current sharing configuration to supply VCCINT. The POLs were externally wired to the board using thick copper mesh in an effort to mitigate effects of contact resistance and interconnect losses. Performance could be improved if the POLs were mounted directly onto the ML510.

The output capacitors work in tandem with the output inductor to filter the inductor ripple current and to source and sink current to meet the load demand during a load step. The output capacitance is implemented as a network of parallel capacitors covering low, mid and high frequency operation. The capacitor ESR and equivalent series inductance (ESI) have a direct impact on the output voltage ripple, output voltage droop under transient loading and loop stability. Ceramic X7R dielectric capacitors are recommended for their thermal and electrical properties, along with their size and cost.

In addition to playing a role in stability and output voltage ripple, the output capacitor bank must be able to absorb the inductor ripple current. The frequency range of capacitors absorbing the ripple current must be rated to handle this ripple current as well.

The input capacitor network sources the trapezoidal current wave through the source terminal of the high side switch. Therefore, the RMS current handling and maximum voltage rating are the main considerations in selecting the input capacitors. The capacitors also absorb the high frequency components of the switching power supply preventing conducted electromagnetic immunity (EMI) from reaching the upstream supply. The input bypass capacitor SRF should be on the order of 10x higher than the switching frequency of the buck converter. Additional high frequency capacitors may be added to further attenuate the high frequency conducted EMI.

Like the output capacitors, ceramic X7R dielectric capacitors are recommended with the added benefit that the X7R capacitors have very low DC voltage de-rating.

In current-mode control, the output inductor is located inside the current loop. Hence, the outer voltage loop consist of a single pole (the filter capacitor), greatly simplifying loop compensation. This is realized by the 56 kΩ / 1.5 nF compensation network shown in *Figure 15*. The transient response may be improved by adding an additional capacitor across the feedback (sense) resistor, if applicable, to boost the crossover frequency and phase margin.

Figure 15. Design Example Showing Two PE99155 POLs in Current Sharing Configuration Driving The ML510

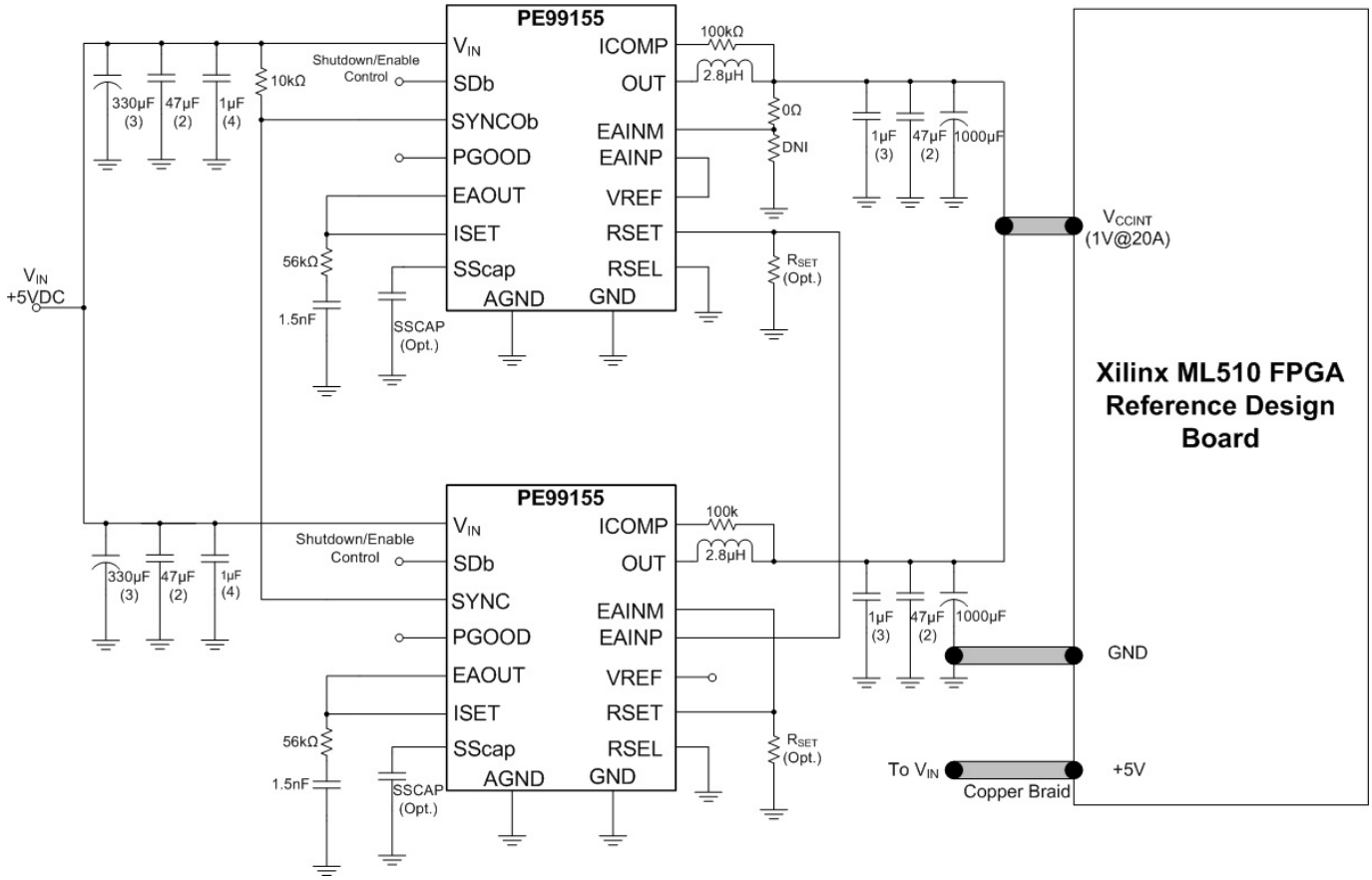


Figure 16. PE99155 Current Sharing Load Transient Response Driving The ML510, 1.5A to 14A Step

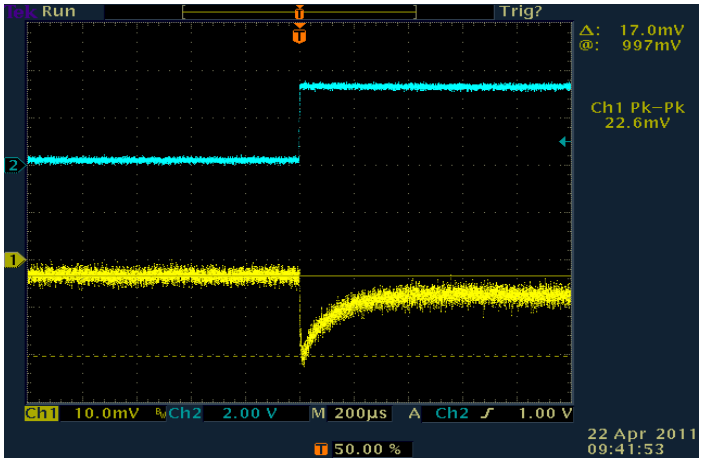


Figure 17. PE99155 Current Sharing Load Transient Response Driving The ML510, 14A to 1.5A Step

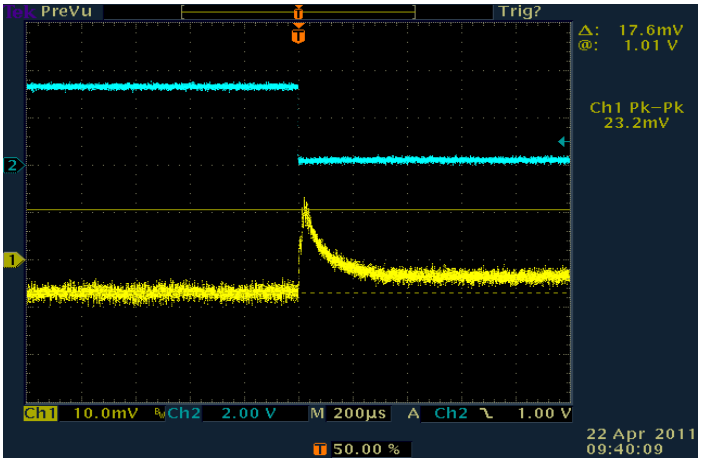
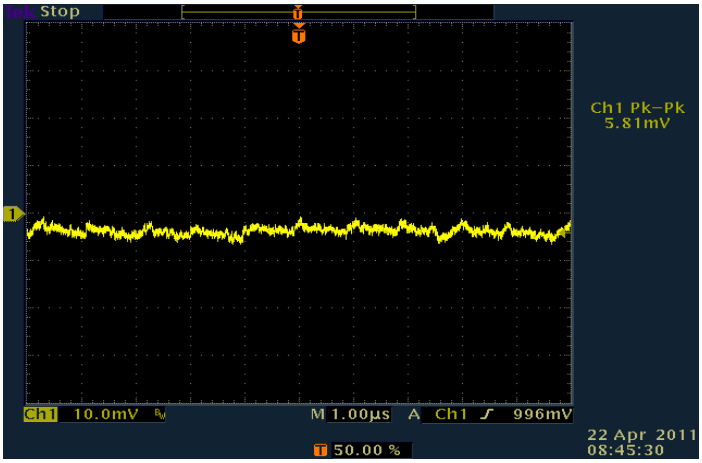


Figure 18. Output Voltage Ripple of Current Sharing PE99155 POLs



Conclusion

The PE9915x highly integrated POL buck regulator products offer power management solutions for the Xilinx radiation tolerant, space-grade Virtex-5QV FPGA as well as other space and satellite applications. The reduced bulk parasitics representative of the UltraCMOS process technology provide immunity to radiation-induced latch-up. Power sequencing can be implemented through PGOOD, enable and soft start features. Adjustable soft-start limits the output voltage ramp rate as well as the inrush current. Synchronous operation enables two or more regulators to be locked together to one frequency thus, eliminating the beat frequency.

Peregrine's ability to combine analog, digital and high performance RF on a single monolithic radiation tolerant die offers huge advantages in reliability, size, weight and cost. Complex solutions realized by large and expensive non-monolithic and hybrid modules can be streamlined using the PE9915x POL buck regulators.

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