

TD99102 Evaluation Kit

TD99102 EVALUATION KIT USER'S GUIDE

This evaluation kit (EVK) is an evaluation system for the TD99102 GaN FET Driver and TDG100E90 GaN FETs. The kit includes one TD99102 integrated circuit (IC), two TDG100E90 FETs, a supply voltage regulator and an input driver.

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1. Features

- Complete evaluation kit for the TD99102 GaN FET driver and the TDG100E90 GaN FETs.
- Includes regulated supply voltage to support the TD99102.
- Includes a buffer for the input signal for the TD99102.

1.1. Kit Contents

- TD99102 / TDG100E90 circuit module.

1.2. Ordering Information

Table 1: Ordering Information

EVK PART NUMBER	DB NUMBER	PACKAGE OPTION
99102D-X00	76939	16-PIN CSP
99102P-X00	76940	16-PIN CLCC

1.3. Documentation

See the device data sheets for TD99102 and the TDG100E90 devices for detailed performance data for these devices.

1.4. TD99102 / TDG100E90 Circuit Module Performance Specification Summary

This section summarizes the performance specifications of the TD99102 / TDG100E90 circuit module.

Table 2: Input Specification Table

Specification	Minimum	Typical	Maximum	Units
Input voltage at 9V_EXT				
9V_EXT to 6V jumper open	7	9	11	V
9V_EXT to 6V jumper shorted	5	5.5	6	V
Input Voltage at INPUT	0	4	5	V
Input Voltage at VIN+	0		48	V
Input frequency at INPUT	1	3	10	MHz
Load Current		3	20	A

2. TD99102 EVK Quick Start Guide

This section provides the step-by-step procedures required to take a new EVK and configure it for operation in a laboratory environment.

2.1. Items needed for EVK setup and Evaluation

- TD99102 / TDG100E90 circuit module
- A DC power supply that can supply 9V and 1A.
- A DC power supply that can supply 100V and 10A.
- A signal generator that can provide up to a 10MHz square wave.
- Oscilloscope

2.2. EVM Connections

This section covers the hardware connections for the EVK. See Figure 1.

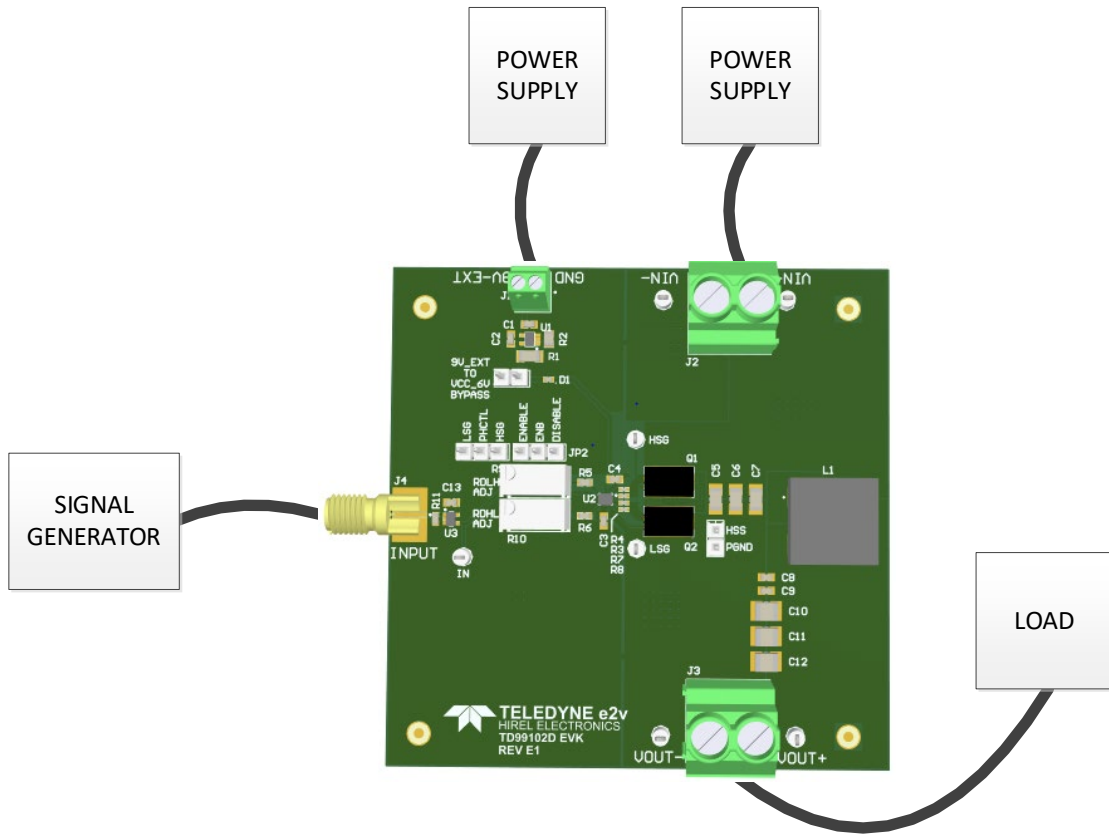


Figure 1: TD99102 Circuit Module Connections to Test Equipment and Load

- The supply voltage for the TD99102 GaN FET Driver connection across 9V-EXT and GND

Attach power supply for the TD99102 GaN FET Driver to the J1 terminal block. The positive wire should be connected to the 9V-EXT terminal block position. The negative wire should be connected to the GND terminal block position. See **Figure 1**. Reference Table 2 to set the supply voltage.

- The supply voltage for the TDG100E90 GaN FET output stage connection across VIN+ and VIN-

Attach power supply for the output stage to the J2 terminal block. The positive wire should be connected to the VIN+ terminal block position. The negative wire should be connected to the VIN- terminal block position. See **Figure 1**. Reference Table 2 to set the supply voltage.

- The PWM input signal for the TD99102 GaN FET Driver connection to the INPUT port

The single-ended pulse width modulation (PWM) input signal is connected to the J4 SMA connector. See **Figure 1**. Reference Table 2 to select the switching frequency.

- The system load connection across VOUT+ and VOUT-

Attach the load to the J3 terminal block. The positive load wire should be connected to the VOUT+ terminal block position. The negative load wire should be connected to the VOUT- terminal block position. See **Figure 1**.

- The TD99102 supply voltage regulator bypass jumper – JP1

The TD99102 supply voltage regulator provides a regulated 6V input to power the device. The regulator can be bypassed by placing a shunt across the JP1 jumper and providing a supply voltage across the 9V-EVT and GND inputs on the J1 terminal block. Reference **Table 2** to set the supply voltage.

- The TD99102 enable jumper – JP2

The TD99102 device is enabled by placing a shunt across the center position and the (-) position on the JP2 jumper. The device is disabled by placing a shunt across the center position and the (+) position on the JP2 jumper.

2.3. Initial Settings Table

This section provides an example setup for the EVK.

Table 3: Initial Setup

Terminal Block / Jumper	Setting	Units
J1	8	V
J2	20	V
J3	10	ohms
J4	4	V
	3	MHz
JP1	open	position
JP2	(-)	position

2.4. Power-up sequence

- Remove the load.
- Enable the signal generator output.
- Turn the 9V-EXT power supply on.
- Turn the VIN+ power supply on.
- Use an oscilloscope to probe the high-side and low-side gate drive signals to inspect the dead-time. Use the R11 (RDLH) and R12 (RDHL) to adjust the dead-time to prevent the signals from overlapping and causing shoot through in the FETs.

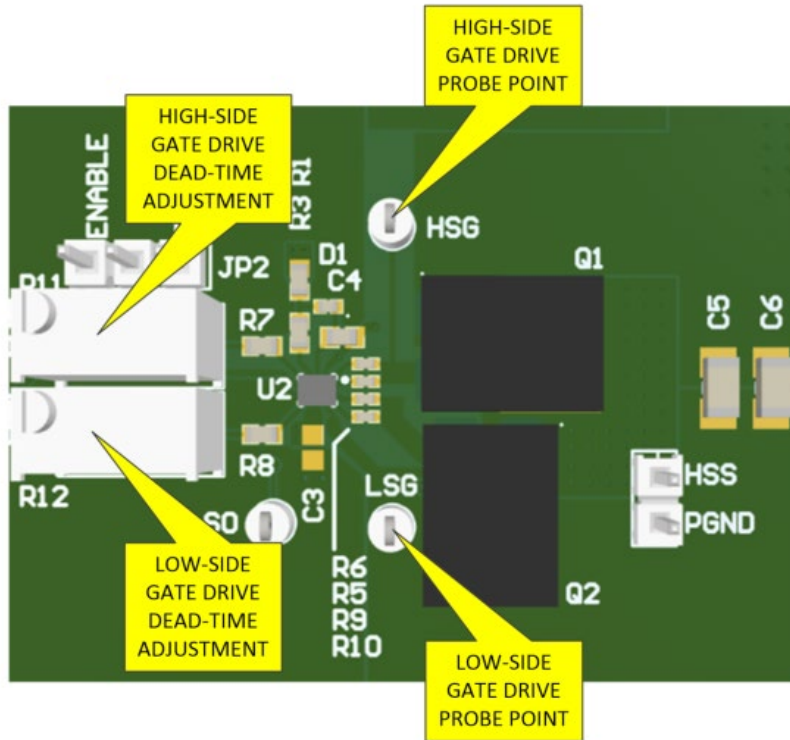


Figure 2: Gate drive dead-time adjustment

- Apply the load.
- Re-check the dead-time and adjust as-needed. Re-check the dead-time after changing the operating frequency or the load and optimize it to improve the output efficiency.

3. Circuit Module Physical Layouts

This section contains the printed-circuit board (PCB) layout, assembly drawings, and schematic for the TD99102 EVK.

3.1. Board Layout

This section shows the dimensions, PCB layers (Figure 3 through Figure 8), and assembly drawing for the TD99102 EVK's.

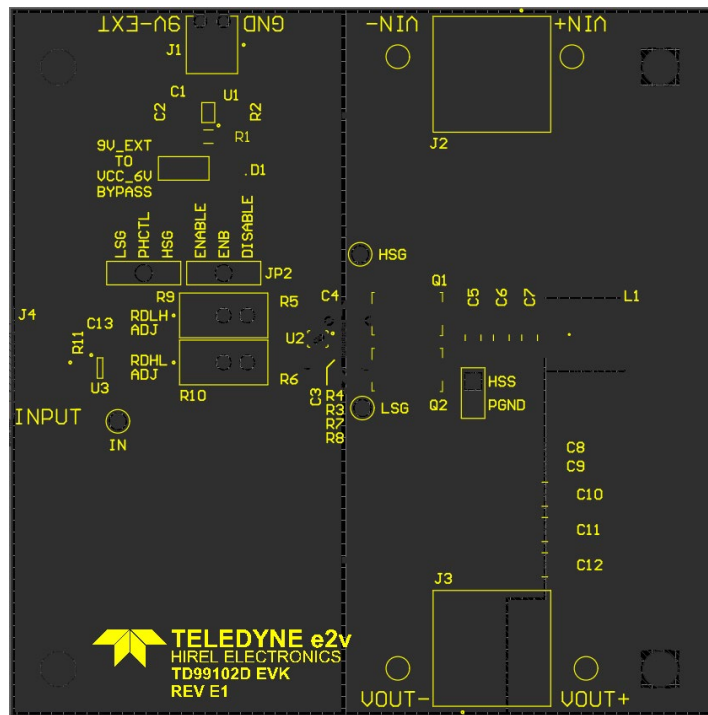


Figure 3: Top Silk Screen

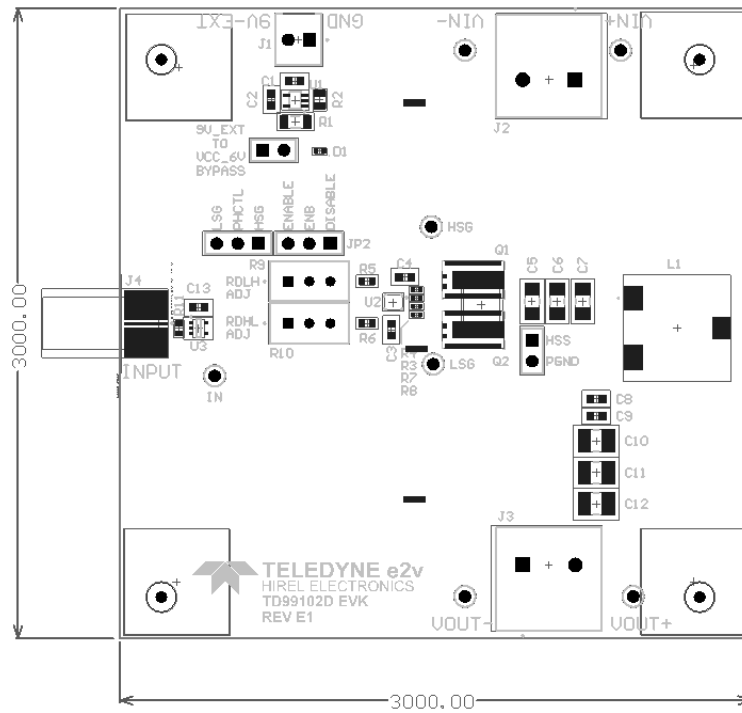


Figure 4: Top Assembly

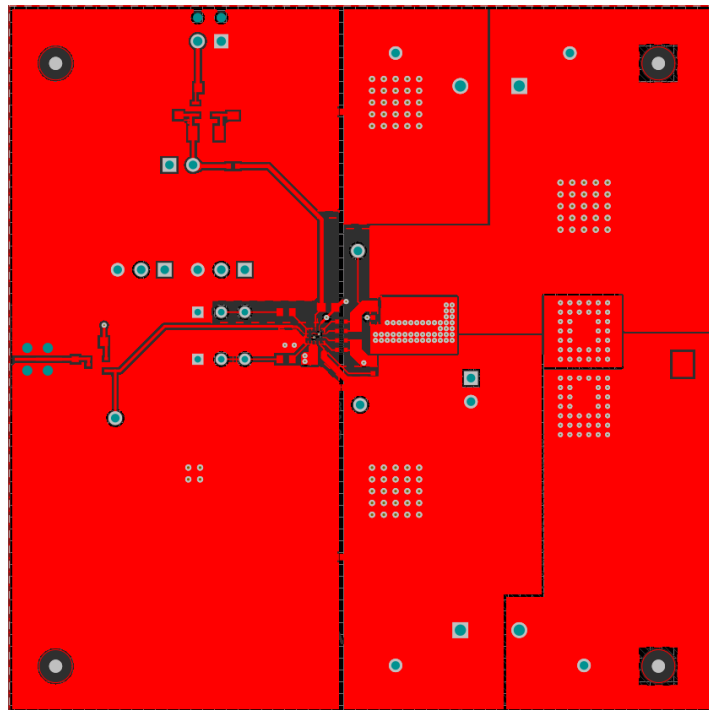


Figure 5: Top Layer

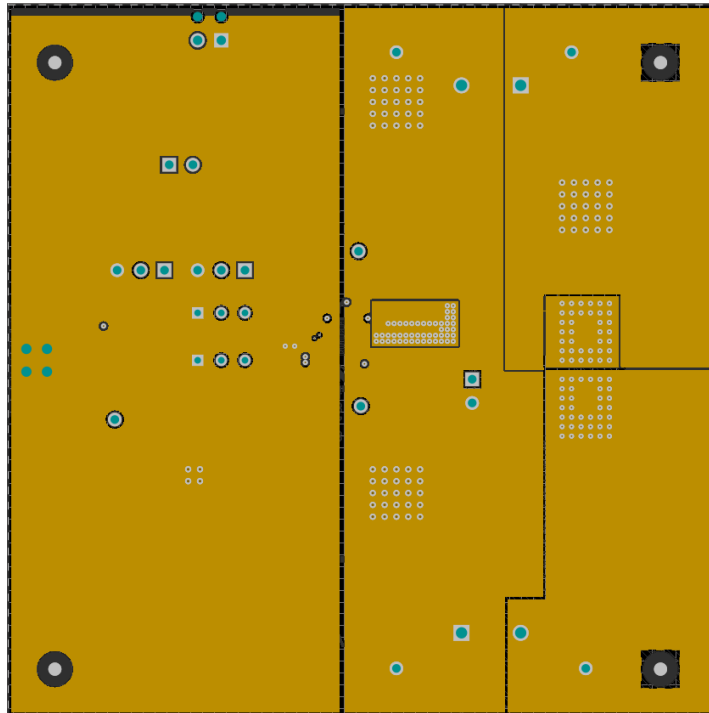


Figure 6: Internal Layer 1

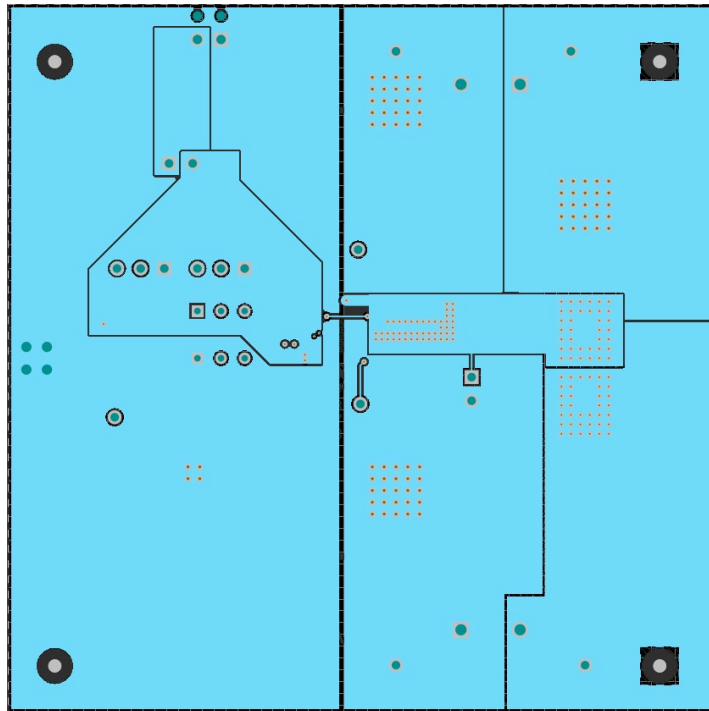


Figure 7: Internal Layer 2

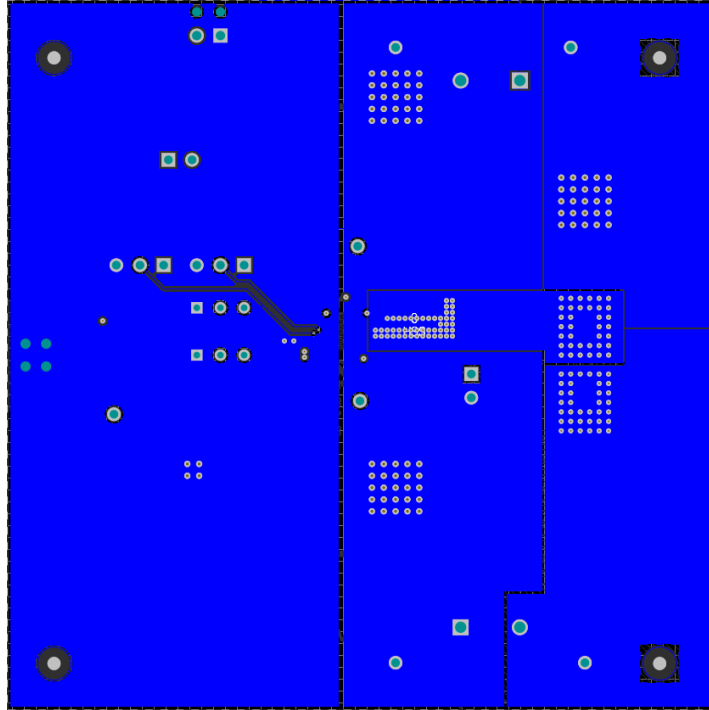


Figure 8: Bottom Layer

TD99102 Evaluation Kit

3.2. Schematic

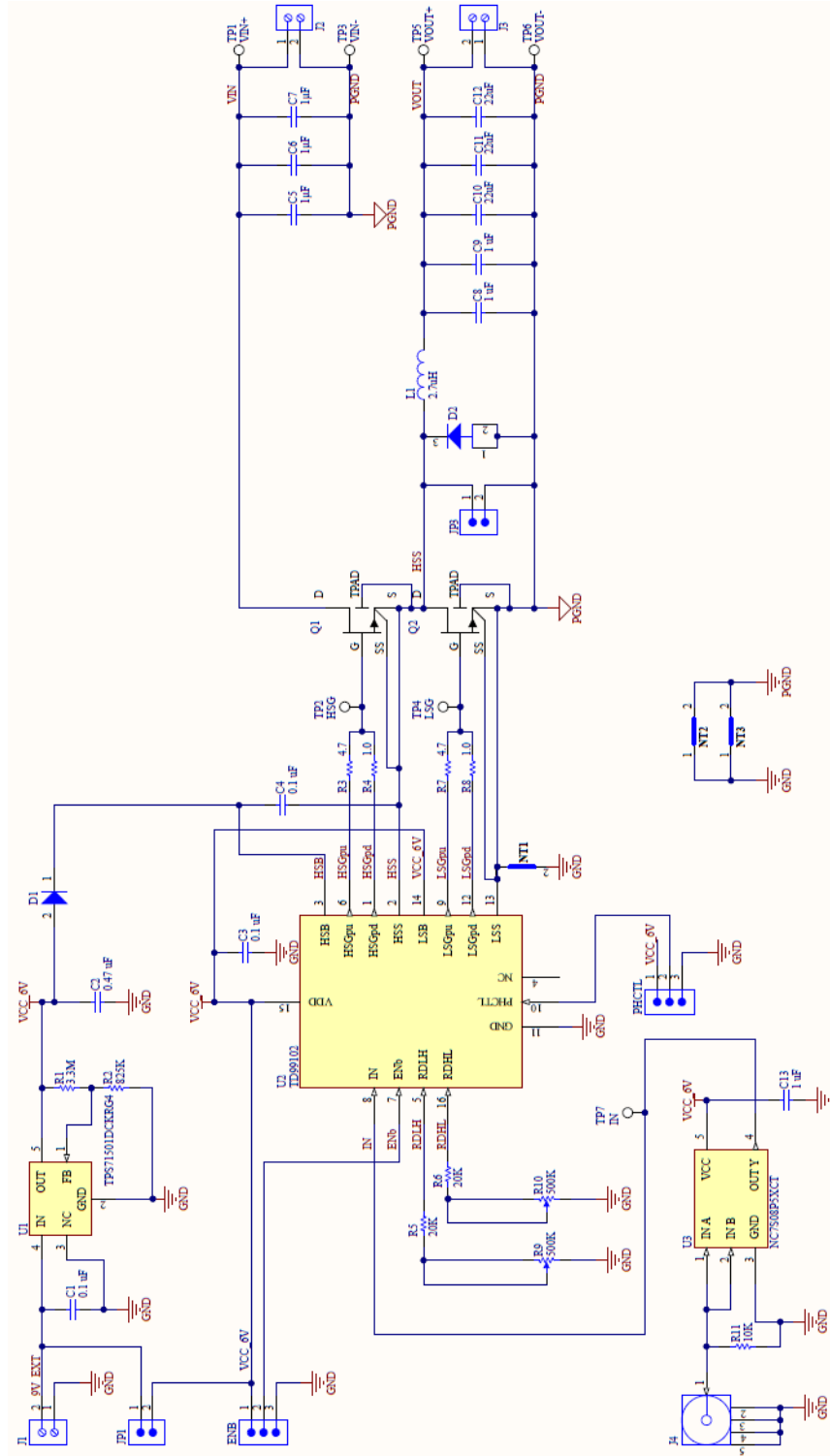


Figure 9: Schematic

4. Bill of Materials

Qty	Designator	Value	Description	Part Number	Size
3	C1, C3, C4	0.1 uF	0.1µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	C1608X7R1H104 K080AE	0603
1	C2	0.47 uF	0.47µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	CGA3E3X7R1H4 74K080AE	0603
3	C5, C6, C7	1µF	1µF ±10% 100V Ceramic Capacitor X7R 1206 (3216 Metric)	GCJ31CR72A105 KA01L	1206
3	C8, C9, C13	1 uF	1µF ±10% 25V Ceramic Capacitor X5R 0603 (1608 Metric)	CGA3E3X5R1E1 05K080AB	0603
3	C10, C11, C12	22uF	22µF ±10% 25V Ceramic Capacitor X5R 1206 (3216 Metric)	CL31A226KAHN NNE	1206
1	D1	BAS70LP-TP	Diode Schottky 70V 70mA (DC) Surface Mount SOD-882	BAS70LP-TP	SOD-882
0	D2	DNI	Mount Schottky Barrier Rectifier, 60 V, 3A, -55 to 150 degC, 3-pin TO-277A,	PDS360-13	TO-277
4	F1, F2, F3, F4		Bumper Square, Tapered 0.500" L x 0.500" W (12.70mm x 12.70mm) Polyurethane Black	SJ-5518	12.7 x 12.7 mm
1	J1		Male2 Position Wire to Board Terminal Block Horizontal with Board 0.100" (2.54mm) Through Hole	1725656	6.2mm x 5.54mm
2	J2, J3		PC Terminal Block, Pitch 6.35 mm, 1 x 2 Position, Height 21.5 mm, Tail Length 5.1 mm, RoHS, Bulk	1714955	19.05mm x 12.5mm
1	J4		SMA High Freq End Launch Jack Receptacle, PCB Mount, 10 MIL Pin, 26.5 GHz, 50 Ohm, -65 to 165 degC, Round Body Radius 6.27 mm, Body Length 9.52 mm, RoHS	142-0761-881	142-0761-881-5
2	JP1, JP3		2 Positions Header Connector 0.100" (2.54mm) Through Hole Gold	TSW-102-26-G-S	TSW-102-26-XX-S
1	JP2, JP4		3 Positions Header Connector 0.100" (2.54mm) Through Hole Gold	TSW-103-07-G-S	TSW-103-07-X-S
1	L1	2.7uH	Fixed Inductors SER1360 High Current 2.7 uH 10 % 13 A	SER1360-272	SER1360

2	Q1, Q2		100 V enhancement mode GaN transistor, 8mohm, 100V, 90A	TDG100E90	7.5mm x 4.6mm
1	R1	3.3M	3.3 MOhms $\pm 0.1\%$ 0.25W, 1/4W Chip Resistor 1206 (3216 Metric)	RG3216P-3304-B-T1	1206
1	R2	825K	Thin Film Resistors - SMD 0805 825Kohm 0.1% 25ppm	ERA-6AEB8253V	0805
2	R3, R7	4.7	RES SMD 4.7 OHM 1% 1/6W 0402	RL0510S-4R7-F	0402
2	R4, R8	1.0	RES SMD 1 OHM 1% 1/6W 0402	RL0510S-1R0-F	0402
2	R5, R6	20K	20 kOhms $\pm 1\%$ 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	ERJ-3EKF2002V	0603
2	R9, R10	500K	3296 - 3/8" Square Trimpot(R) Trimming Potentiometer, 500 KOhm, +/- 10%, 0.5 W, -55 to 125 degC, 3-Pin THD, RoHS, Tube	3296W-1-504	9.53mm x 4.83mm
1	R11	10K	10 kOhms $\pm 1\%$ 0.1W, 1/10W Chip Resistor 0603 (1608 Metric)	ERJ-3EKF1002V	0603
2	SH-JP1, SH-JP2		Shunt, 100mil, Gold plated, Black	QPC02SXGN-RC	Shunt
7	TP1, TP2, TP3, TP4, TP5, TP6, TP7		Test Point, White, 1-Pin THD, RoHS, Bulk	5002	2.54mm x 4.57mm
1	U1	TPS71501DCKRG4	Single Output LDO, 50 mA, Adjustable 1.2 to 15 V Output, 3 to 24 V Input, 5-pin SC70 (DCK), -40 to 125 degC, Green (RoHS & no Sb/Br)	TPS71501DCKRG4	DCK5
1	U2	TD99102D	GaN FET Driver	TD99102D	
1	U3	NC7S08P5XCT	AND Gate IC 1 Channel SC-70-5	NC7S08P5X	SC70-5

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