Qormino QT1040
Qormino Integrated Multicore Communications Processor with DDR3L

Datasheet Preliminary DS1183

FEATURES

- e5500 cores built on Power Architecture® technology,
  - QT1040 has four cores and QT1020 has two cores
  - Each core with a private 256KB L2 cache
  - 1GB DDR3L with ECC
- 256 KB shared L3 CoreNet platform cache (CPC)
- Hierarchical interconnect fabric
  - CoreNet Coherency manager supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - 150Gbps coherent read bandwidth
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution
  - Queue management for scheduling, packet sequencing, and congestion management
  - Hardware buffer management for buffer allocation and de-allocation
  - Cryptography Acceleration
  - RegEx Pattern Matching Acceleration
  - IEEE Std 1588™ support
- Integrated 8-port Gigabit Ethernet switch
  - 8K MAC addresses, 4K VLANs
  - Static Address provisioning
  - Dynamic learning of MAC addresses and aging
  - Policing with storm control and MC/BC protection
  - Link aggregation (IEEE Std 802.3ad)
  - Spanning Tree Protocol (STP, RSTP and MSTP)
  - Access Control List
  - VLAN editing, translation and remarking
  - Hierarchical QoS with DWRR scheduling
- Parallel Ethernet interfaces
  - Up to two RGMII interface
  - One MII interface
- Eight SerDes lanes for high-speed peripheral interfaces
  - Four PCI Express 2.0 controllers
  - Two Serial ATA (SATA 3Gb/s) controllers
  - Up to two QSGMII interface
  - Up to six SGMII interface supporting 1000 Mbps
  - Supports 1000Base-KX
- Additional peripheral interfaces
  - Two high-speed USB 2.0 controllers with integrated PHY
  - Enhanced secure digital host controller with support for high capacity memory card (SD/eSDHC/eMMC)
  - Enhanced Serial peripheral interface (eSPI)
  - Four I2C controllers
  - Two DUARTs
  - Integrated flash controller supporting NAND and NOR flash
  - Display interface unit (DIU) with 12-bit dual data rate
  - TDM Interface
  - Four GPIO controllers supporting up to 109 general purpose I/O signals
  - Two 8-channel DMA engines
  - Multicore programmable interrupt controller (MPIC)
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals
  - Serial DMA channel for receive and transmit on all serial channels
  - Two universal communication controllers, supporting TDM, HDLC and UART
- 878 FC-PBGA package, 25 mm × 38 mm

OVERVIEW

The QT1040 Qormino advanced multicore processor combines four 64-bit ISA Power Architecture™ processor cores with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also simplifying board design.

This figure shows the block diagram of the chip.

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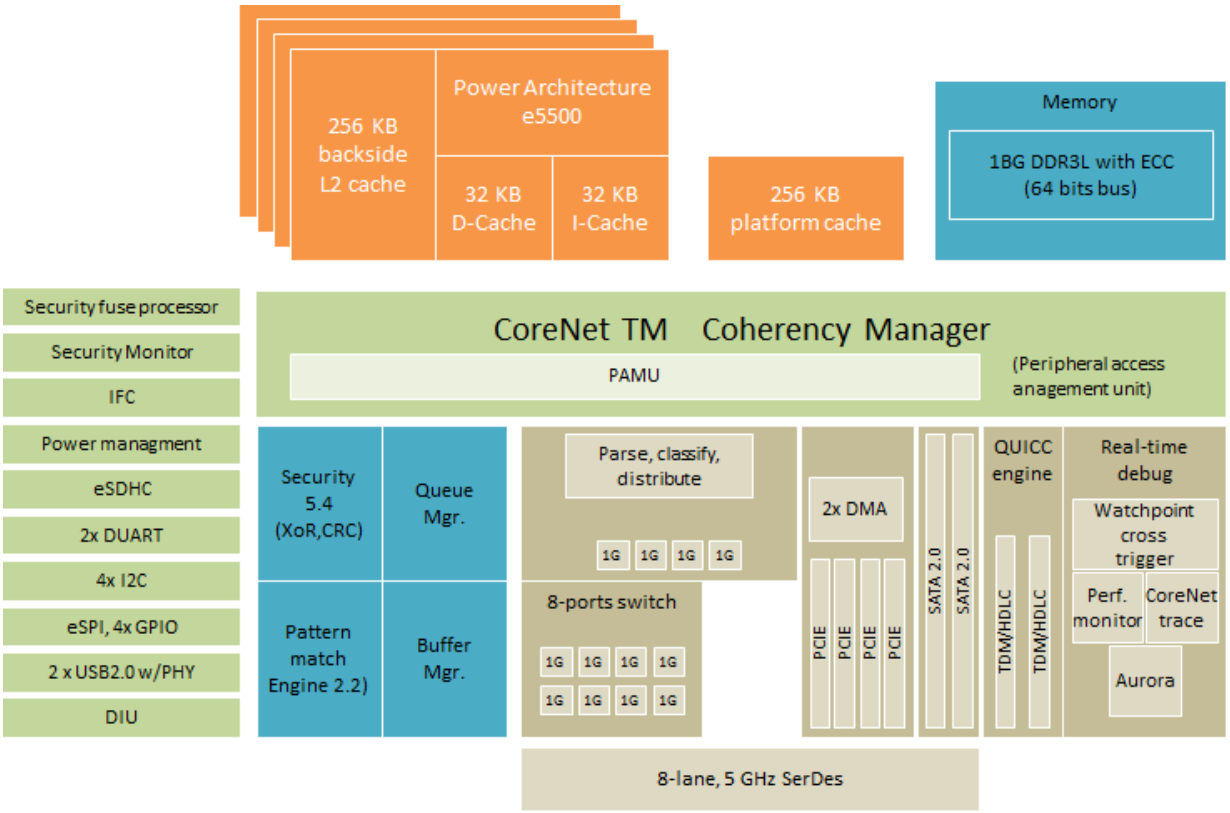
1. BLOCK DIAGRAM

Figure 1-1. QT1040 Block diagram



2. PIN ASSIGNMENTS

2.1 780 ball layout diagrams

This figure shows the complete view of the QT1040 ball map diagram. Figure 2-2, Figure 2-3, Figure 2-4, and Figure 2-5 show quadrant views.

Figure 2-1. Complete BGA Map for the QT1040

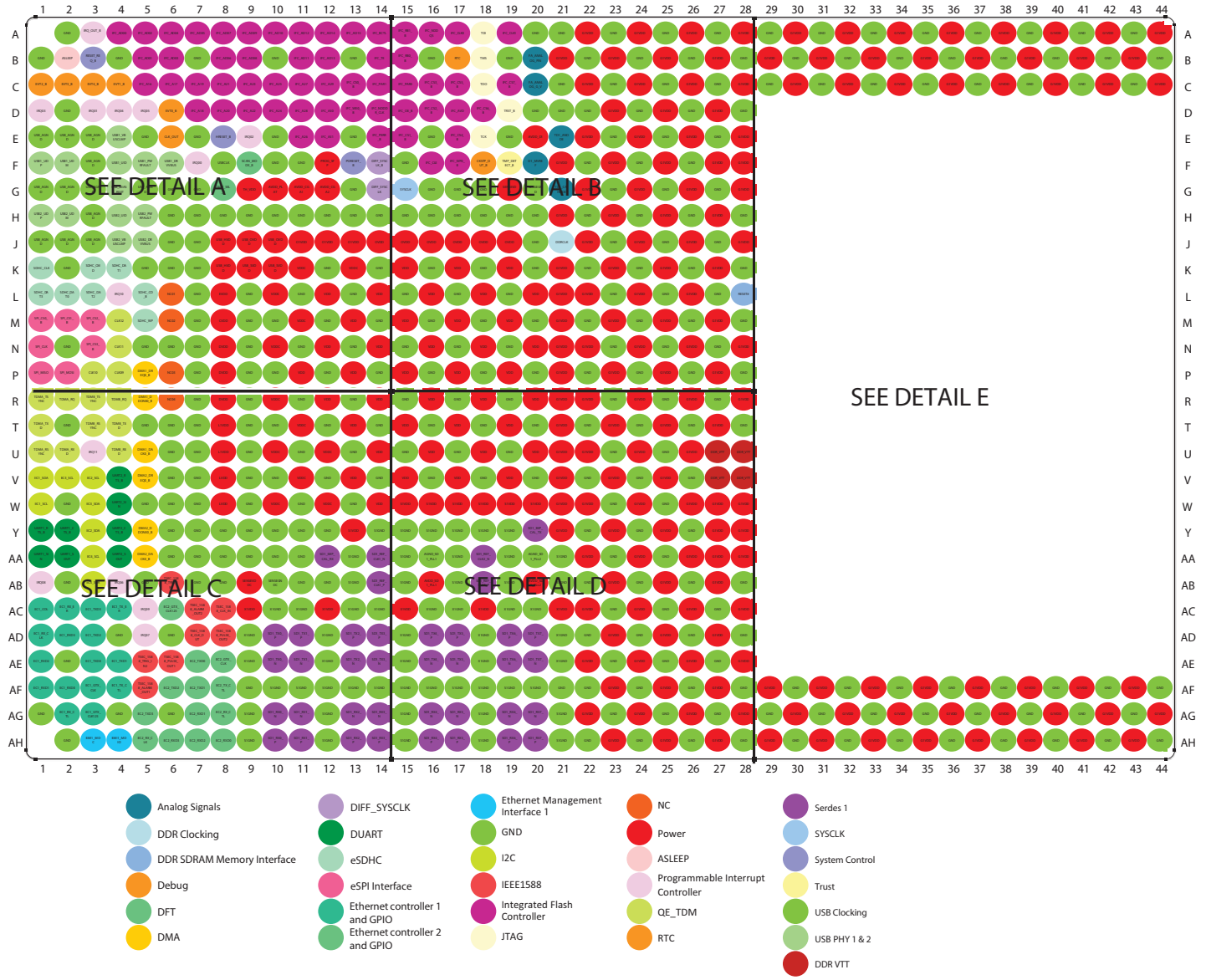


Figure 2-2. Detail A

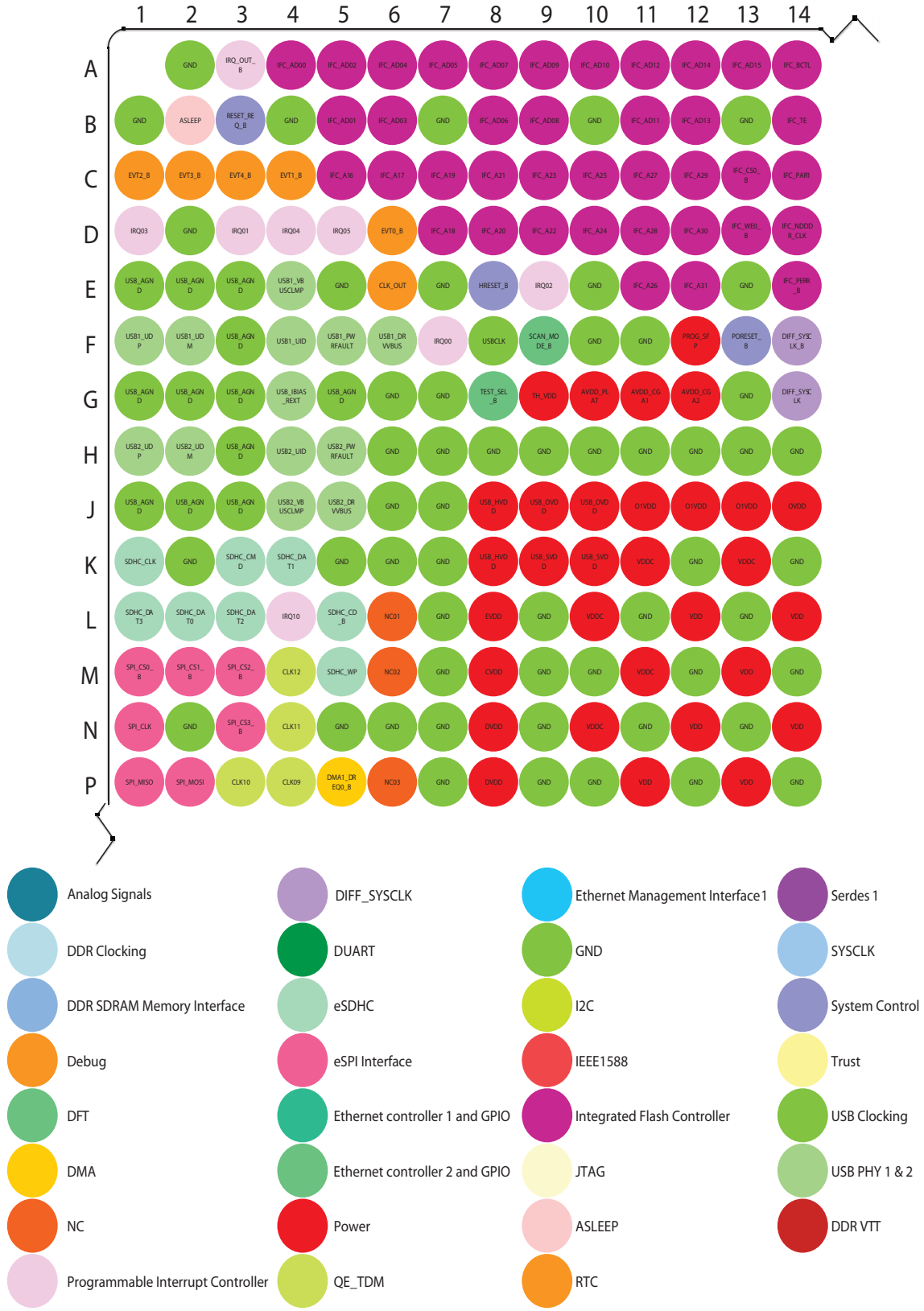


Figure 2-3. Detail B

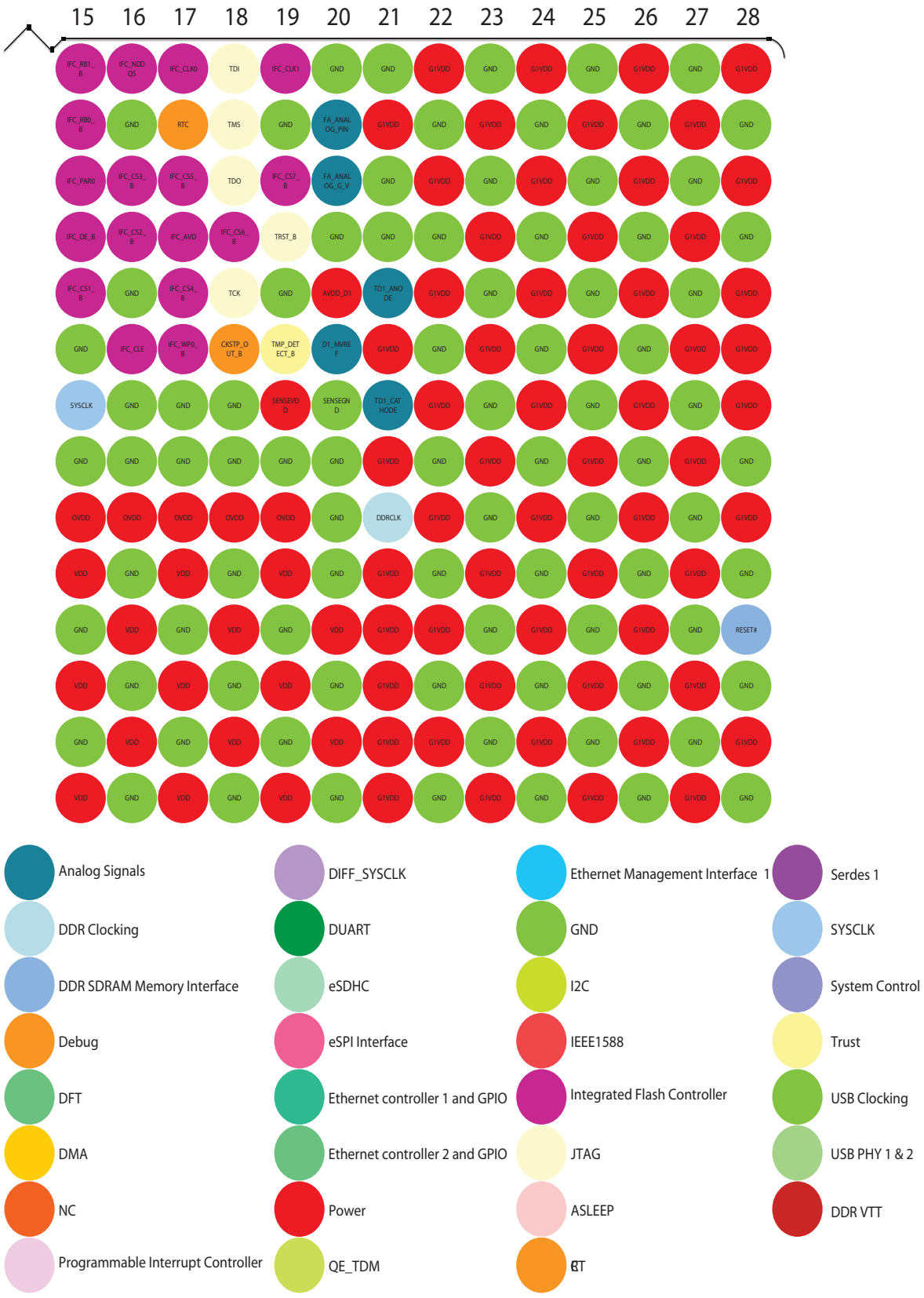


Figure 2-4. Detail C

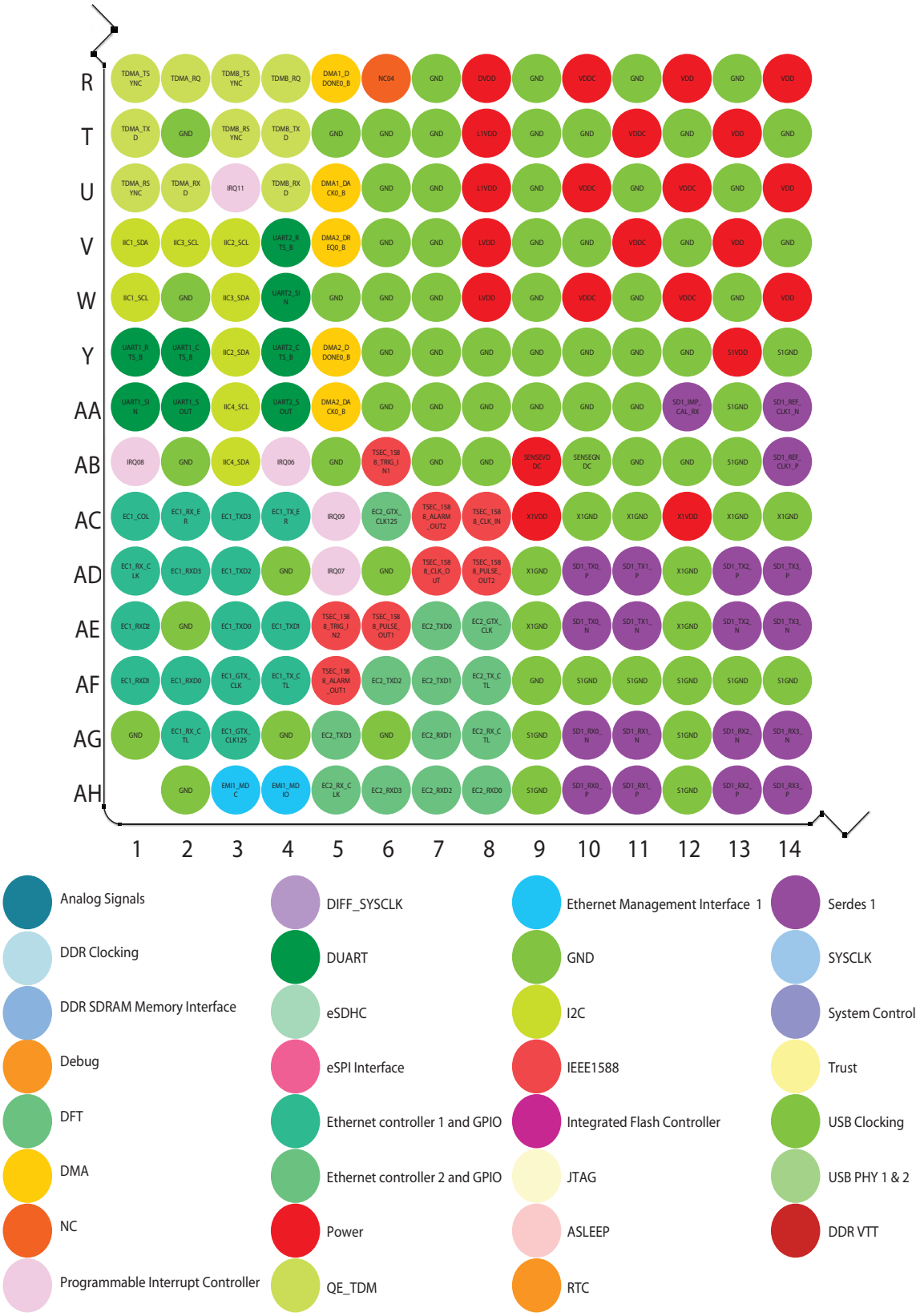


Figure 2-5. Detail D

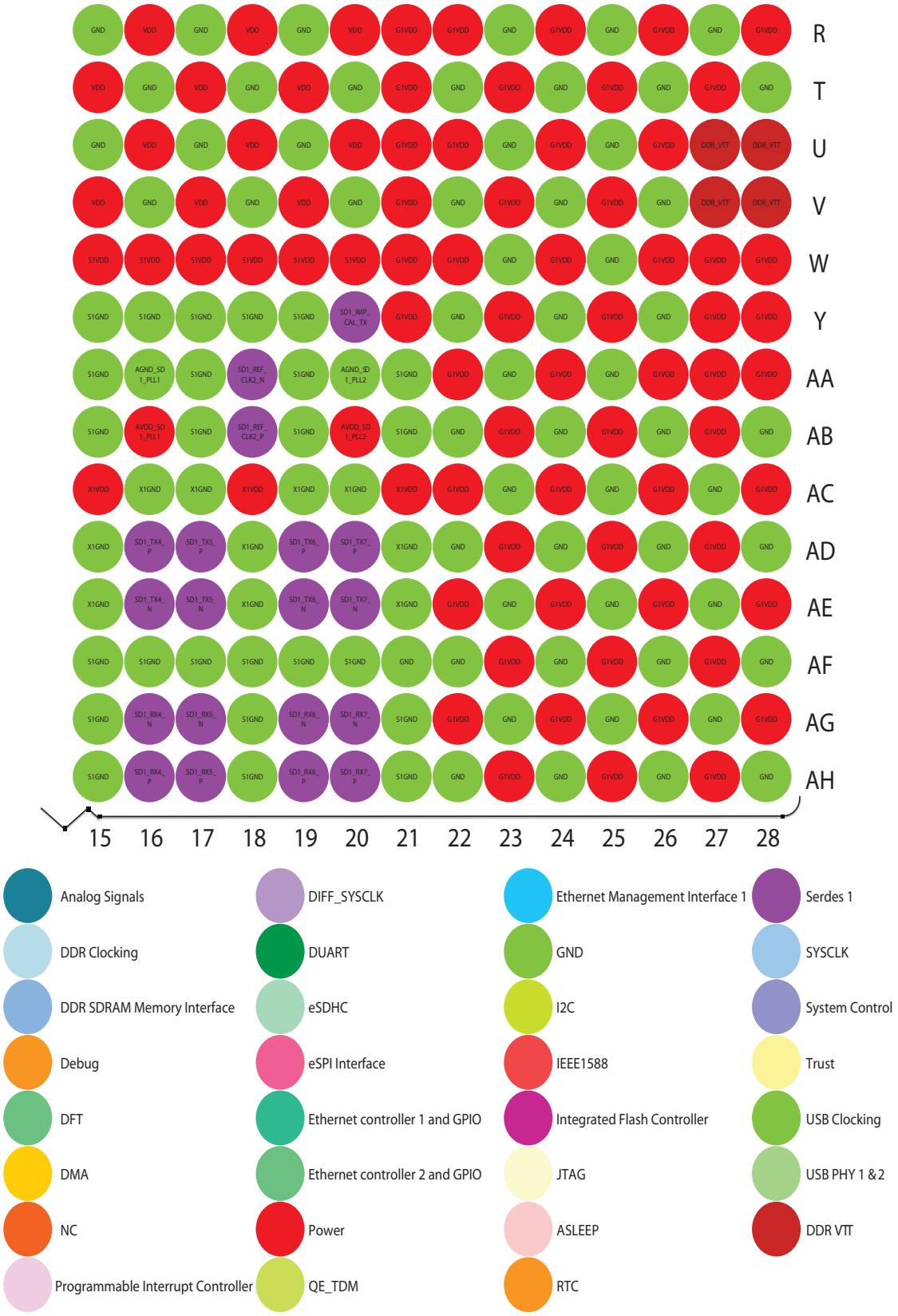
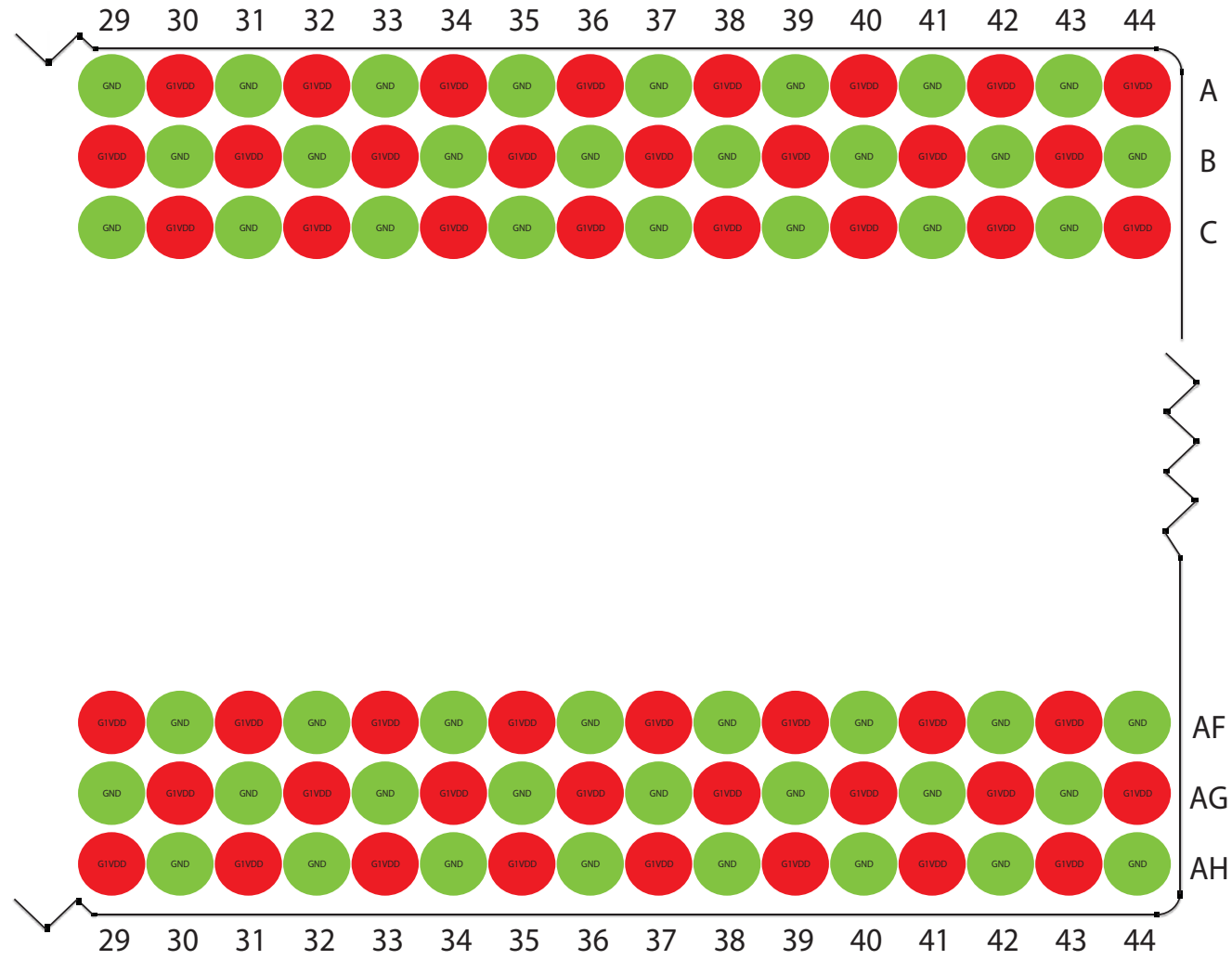
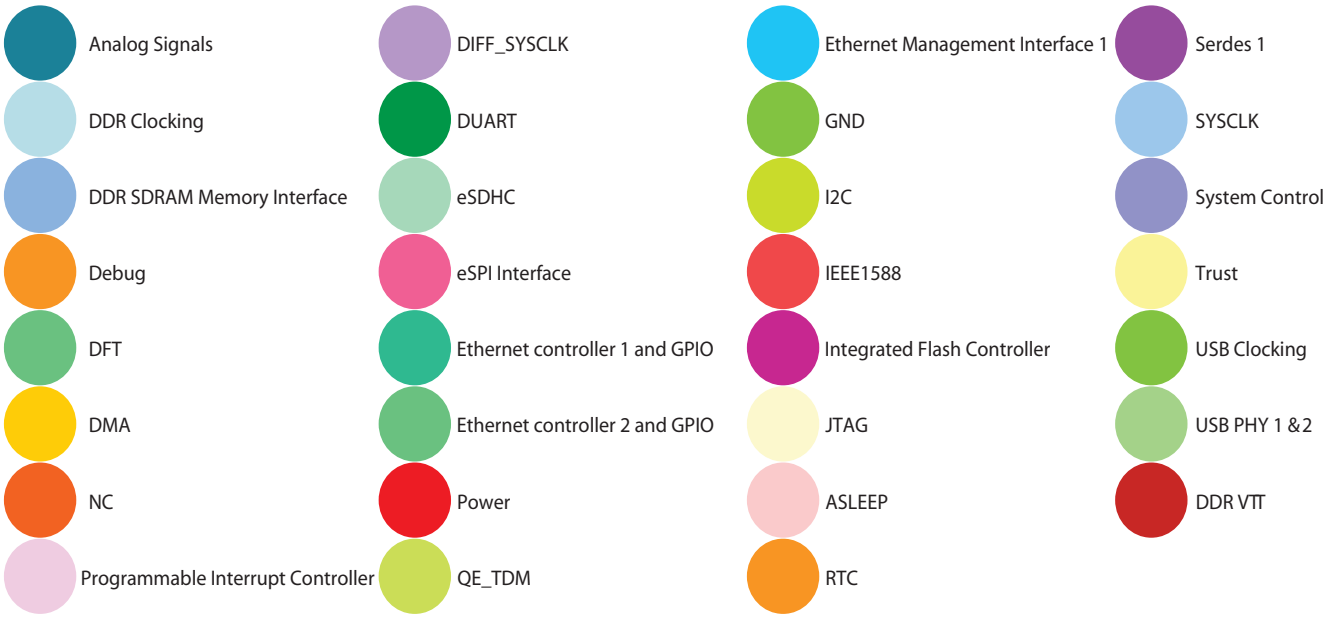


Figure 2-6. Detail E





2.2 Pinout list

This table provides the pinout listing for the QT1040 by bus. Primary functions are **bolded** in the table.

Table 2-1. Pinout List

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
RESET#	DDR Reset#	L28	I	G1VDD	–
Integrated Flash Controller					
IFC_A16	IFC Address	C5	O	OVDD	(1)(5)
IFC_A17	IFC Address	C6	O	OVDD	(1)(5)
IFC_A18	IFC Address	D7	O	OVDD	(1)(5)
IFC_A19	IFC Address	C7	O	OVDD	(1)(5)
IFC_A20	IFC Address	D8	O	OVDD	(1)(5)
IFC_A21/cfg_dram_type	IFC Address	C8	O	OVDD	(1)(4)
IFC_A22	IFC Address	D9	O	OVDD	(1)
IFC_A23	IFC Address	C9	O	OVDD	(1)
IFC_A24	IFC Address	D10	O	OVDD	(1)
IFC_A25/GPIO2_25/ IFC_WP1_B	IFC Address	C10	O	OVDD	(1)
IFC_A26/GPIO2_26/ IFC_WP2_B	IFC Address	E11	O	OVDD	(1)
IFC_A27/GPIO2_27/ IFC_WP3_B	IFC Address	C11	O	OVDD	(1)
IFC_A28/GPIO2_28	IFC Address	D11	O	OVDD	(1)
IFC_A29/GPIO2_29/ IFC_RB2_B	IFC Address	C12	O	OVDD	(1)
IFC_A30/GPIO2_30/ IFC_RB3_B	IFC Address	D12	O	OVDD	(1)
IFC_A31/GPIO2_31/ IFC_RB4_B	IFC Address	E12	O	OVDD	(1)
IFC_AD00/cfg_gpinput0	IFC Address / Data	A4	IO	OVDD	(4)
IFC_AD01/cfg_gpinput1	IFC Address / Data	B5	IO	OVDD	(4)
IFC_AD02/cfg_gpinput2	IFC Address / Data	A5	IO	OVDD	(4)
IFC_AD03/cfg_gpinput3	IFC Address / Data	B6	IO	OVDD	(4)
IFC_AD04/cfg_gpinput4	IFC Address / Data	A6	IO	OVDD	(4)
IFC_AD05/cfg_gpinput5	IFC Address / Data	A7	IO	OVDD	(4)
IFC_AD06/cfg_gpinput6	IFC Address / Data	B8	IO	OVDD	(4)
IFC_AD07/cfg_gpinput7	IFC Address / Data	A8	IO	OVDD	(4)
IFC_AD08/cfg_rcw_src0	IFC Address / Data	B9	IO	OVDD	(4)
IFC_AD09/cfg_rcw_src1	IFC Address / Data	A9	IO	OVDD	(4)
IFC_AD10/cfg_rcw_src2	IFC Address / Data	A10	IO	OVDD	(4)
IFC_AD11/cfg_rcw_src3	IFC Address / Data	B11	IO	OVDD	(4)
IFC_AD12/cfg_rcw_src4	IFC Address / Data	A11	IO	OVDD	(4)
IFC_AD13/cfg_rcw_src5	IFC Address / Data	B12	IO	OVDD	(4)
IFC_AD14/cfg_rcw_src6	IFC Address / Data	A12	IO	OVDD	(4)
IFC_AD15/cfg_rcw_src7	IFC Address / Data	A13	IO	OVDD	(4)

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AVD	IFC Address Valid	D17	O	OV_{DD}	(1)(5)
IFC_BCTL	IFC Buffer control	A14	O	OV_{DD}	(1)
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable	F16	O	OV_{DD}	(1)(4)
IFC_CLK0	IFC Clock	A17	O	OV_{DD}	(1)
IFC_CLK1	IFC Clock	A19	O	OV_{DD}	(1)
IFC_CS0_B	IFC Chip Select	C13	O	OV_{DD}	(1)(6)
IFC_CS1_B/GPIO2_10	IFC Chip Select	E15	O	OV_{DD}	(1)(6)
IFC_CS2_B/GPIO2_11	IFC Chip Select	D16	O	OV_{DD}	(1)(6)
IFC_CS3_B/GPIO2_12	IFC Chip Select	C16	O	OV_{DD}	(1)(6)
IFC_CS4_B/GPIO1_09	IFC Chip Select	E17	O	OV_{DD}	(1)(6)
IFC_CS5_B/GPIO1_10	IFC Chip Select	C17	O	OV_{DD}	(1)(6)
IFC_CS6_B/GPIO1_11	IFC Chip Select	D18	O	OV_{DD}	(1)(6)
IFC_CS7_B/GPIO1_12	IFC Chip Select	C19	O	OV_{DD}	(1)(6)
IFC_NDDDR_CLK	IFC NAND DDR Clock	D14	O	OV_{DD}	(1)
IFC_NDDQS	IFC DQS Strobe	A16	IO	OV_{DD}	–
IFC_OE_B/cfg_eng_use1	IFC Output Enable	D15	O	OV_{DD}	(1)(22)
IFC_PAR0/GPIO2_13	IFC Address & Data Parity	C15	IO	OV_{DD}	–
IFC_PAR1/GPIO2_14	IFC Address & Data Parity	C14	IO	OV_{DD}	–
IFC_PERR_B/GPIO2_15	IFC Parity Error	E14	I	OV_{DD}	(1)(6)
IFC_RB2_B/**IFC_A29**/ GPIO2_29	IFC Ready / Busy CS 2	C12	I	OV_{DD}	(1)
IFC_RB3_B/**IFC_A30**/ GPIO2_30	IFC Ready / Busy CS 3	D12	I	OV_{DD}	(1)
IFC_RB4_B/**IFC_A31**/ GPIO2_31	IFC Ready / Busy CS 4	E12	I	OV_{DD}	(1)
IFC_RB0_B	IFC Ready / Busy CS0	B15	I	OV_{DD}	(6)
IFC_RB1_B	IFC Ready / Busy CS1	A15	I	OV_{DD}	(6)
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	B14	O	OV_{DD}	(1)(4)
IFC_WE0_B/cfg_eng_use0	IFC Write Enable	D13	O	OV_{DD}	(1)(22)
IFC_WP1_B/**IFC_A25**/ GPIO2_25	IFC Write Protect	C10	O	OV_{DD}	(1)
IFC_WP2_B/**IFC_A26**/ GPIO2_26	IFC Write Protect	E11	O	OV_{DD}	(1)
IFC_WP3_B/**IFC_A27**/ GPIO2_27	IFC Write Protect	C11	O	OV_{DD}	(1)
IFC_WP0_B/cfg_eng_use2	IFC Write Protect	F17	O	OV_{DD}	(1)(22)
DUART					
UART1_CTS_B/GPIO1_21/ UART3_SIN	Clear To Send	Y2	I	DV_{DD}	(1)
UART1_RTS_B/GPIO1_19/ UART3_SOUT	Ready to Send	Y1	O	DV_{DD}	(1)
UART1_SIN/GPIO1_17	Receive Data	AA1	I	DV_{DD}	(1)
UART1_SOUT/GPIO1_15	Transmit Data	AA2	O	DV_{DD}	(1)
UART2_CTS_B/GPIO1_22/ UART4_SIN	Clear To Send	Y4	I	DV_{DD}	(1)
UART2_RTS_B/GPIO1_20/ UART4_SOUT	Ready to Send	V4	O	DV_{DD}	(1)

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART2_SIN/GPIO1_18	Receive Data	W4	I	DV_{DD}	(1)
UART2_SOUT/GPIO1_16	Transmit Data	AA4	O	DV_{DD}	(1)
UART3_SIN/**UART1_CTS_B**/ GPIO1_21	Receive Data	Y2	I	DV_{DD}	(1)
UART3_SOUT/**UART1_RTS_B**/GPIO1_19	Transmit Data	Y1	O	DV_{DD}	(1)
UART4_SIN/**UART2_CTS_B**/ GPIO1_22	Receive Data	Y4	I	DV_{DD}	(1)
UART4_SOUT/**UART2_RTS_B**/GPIO1_20	Transmit Data	V4	O	DV_{DD}	(1)
I2C					
IIC1_SCL	Serial Clock (supports PBL)	W1	IO	DV_{DD}	(7)(8)
IIC1_SDA	Serial Data (supports PBL)	V1	IO	DV_{DD}	(7)(8)
IIC2_SCL	Serial Clock	V3	IO	DV_{DD}	(7)(8)
IIC2_SDA	Serial Data	Y3	IO	DV_{DD}	(7)(8)
eSPI Interface					
SPI_CLK	SPI Clock	N1	O	CV_{DD}	(1)
SPI_CS0_B/GPIO2_00/ SDHC_DAT4	SPI Chip Select	M1	O	CV_{DD}	(1)
SPI_CS1_B/GPIO2_01/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	M2	O	CV_{DD}	(1)
SPI_CS2_B/GPIO2_02/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	M3	O	CV_{DD}	(1)
SPI_CS3_B/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR/ SDHC_CLK_SYNC_OUT	SPI Chip Select	N3	O	CV_{DD}	(1)
SPI_MISO	Master In Slave Out	P1	I	CV_{DD}	(1)
SPI_MOSI	Master Out Slave In	P2	IO	CV_{DD}	–
Programmable Interrupt Controller					
IRQ00	External Interrupt	F7	I	$O1V_{DD}$	(1)
IRQ01	External Interrupt	D3	I	$O1V_{DD}$	(1)
IRQ02	External Interrupt	E9	I	$O1V_{DD}$	(1)
IRQ03/GPIO1_23/SDHC_VS	External Interrupt	D1	I	$O1V_{DD}$	(1)
IRQ04/GPIO1_24	External Interrupt	D4	I	$O1V_{DD}$	(1)
IRQ05/GPIO1_25	External Interrupt	D5	I	$O1V_{DD}$	(1)
IRQ06/GPIO1_26	External Interrupt	AB4	I	$L1V_{DD}$	(1)
IRQ07/GPIO1_27	External Interrupt	AD5	I	$L1V_{DD}$	(1)
IRQ08/GPIO1_28	External Interrupt	AB1	I	$L1V_{DD}$	(1)
IRQ09/GPIO1_29	External Interrupt	AC5	I	$L1V_{DD}$	(1)
IRQ10/GPIO1_30/ SDHC_CLK_SYNC_IN	External Interrupt	L4	I	CV_{DD}	(1)
IRQ11/GPIO1_31	External Interrupt	U3	I	DV_{DD}	(1)
IRQ_OUT_B/EVT9_B	Interrupt Output	A3	O	$O1V_{DD}$	(1)(6)(7)
Trust					
TMP_DETECT_B	Tamper Detect	F19	I	OV_{DD}	(1)
System Control					

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
HRESET_B	Hard Reset	E8	IO	O1VDD	(7)27
PORESET_B	Power On Reset	F13	I	O1VDD	(26)
RESET_REQ_B	Reset Request (POR or Hard)	B3	O	O1VDD	(1)(5)
Power Management					
ASLEEP/GPO1_13	Asleep	B2	O	O1VDD	(1)
SYSCLK					
SYSCLK	System Clock	G15	I	O1VDD	(17)
DDR Clocking					
DDRCLK	DDR Controller Clock	J21	I	OVDD	(17)
RTC					
RTC/GPIO1_14	Real Time Clock	B17	I	OVDD	(1)
Debug					
CKSTP_OUT_B	Checkstop Out	F18	O	OVDD	(1)(6)(7)
CLK_OUT	Clock Out	E6	O	O1VDD	–
EVT5_B/**IIC4_SCL**/GPIO4_02/ DIU_HSYNC	Event 5	AA3	IO	DVDD	–
EVT6_B/**IIC4_SDA**/GPIO4_03/ DIU_VSYNC	Event 6	AB3	IO	DVDD	–
EVT7_B/**DMA2_DACK0_B**/ GPIO4_08/TDM_RFS	Event 7	AA5	IO	DVDD	–
EVT8_B/**DMA2_DDONE0_B**/ GPIO4_09/TDM_RCK	Event 8	Y5	IO	DVDD	–
EVT9_B/**IRQ_OUT_B**	Event 9	A3	IO	O1VDD	–
EVT0_B	Event 0	D6	IO	O1VDD	(9)
EVT1_B	Event 1	C4	IO	O1VDD	–
EVT2_B	Event 2	C1	IO	O1VDD	(6)(22)
EVT3_B	Event 3	C2	IO	O1VDD	–
EVT4_B	Event 4	C3	IO	O1VDD	–
DFT					
SCAN_MODE_B	Reserved	F9	I	O1VDD	(10)
TEST_SEL_B	Reserved	G8	I	O1VDD	(23)
JTAG					
TCK	Test Clock	E18	I	OVDD	–
TDI	Test Data In	A18	I	OVDD	(9)
TDO	Test Data Out	C18	O	OVDD	–
TMS	Test Mode Select	B18	I	OVDD	(9)
TRST_B	Test Reset	D19	I	OVDD	(9)
Analog Signals					
D1_MVREF	SSTL Reference Voltage	F20	IO	G1VDD/2	–
FA_ANALOG_G_V	Reserved for internal use only	C20	IO	–	(15)
FA_ANALOG_PIN	Reserved for internal use only	B20	IO	–	(15)

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TD1_ANODE	Thermal diode anode	E21	IO		(19)
TD1_CATHODE	Thermal diode cathode	G21	IO		(19)
Serdes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	AA12	I	S1VDD	(11)
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	X1VDD	(16)
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AA14	I	S1VDD	–
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AB14	I	S1VDD	–
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AA18	I	S1VDD	–
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	S1VDD	–
SD1_RX0_N	SerDes Receive Data (negative)	AG10	I	S1VDD	–
SD1_RX0_P	SerDes Receive Data (positive)	AH10	I	S1VDD	–
SD1_RX1_N	SerDes Receive Data (negative)	AG11	I	S1VDD	–
SD1_RX1_P	SerDes Receive Data (positive)	AH11	I	S1VDD	–
SD1_RX2_N	SerDes Receive Data (negative)	AG13	I	S1VDD	–
SD1_RX2_P	SerDes Receive Data (positive)	AH13	I	S1VDD	–
SD1_RX3_N	SerDes Receive Data (negative)	AG14	I	S1VDD	–
SD1_RX3_P	SerDes Receive Data (positive)	AH14	I	S1VDD	–
SD1_RX4_N	SerDes Receive Data (negative)	AG16	I	S1VDD	–
SD1_RX4_P	SerDes Receive Data (positive)	AH16	I	S1VDD	–
SD1_RX5_N	SerDes Receive Data (negative)	AG17	I	S1VDD	–
SD1_RX5_P	SerDes Receive Data (positive)	AH17	I	S1VDD	–
SD1_RX6_N	SerDes Receive Data (negative)	AG19	I	S1VDD	–
SD1_RX6_P	SerDes Receive Data (positive)	AH19	I	S1VDD	–
SD1_RX7_N	SerDes Receive Data (negative)	AG20	I	S1VDD	–
SD1_RX7_P	SerDes Receive Data (positive)	AH20	I	S1VDD	–
SD1_TX0_N	SerDes Transmit Data (negative)	AE10	O	X1VDD	–
SD1_TX0_P	SerDes Transmit Data (positive)	AD10	O	X1VDD	–
SD1_TX1_N	SerDes Transmit Data (negative)	AE11	O	X1VDD	–
SD1_TX1_P	SerDes Transmit Data (positive)	AD11	O	X1VDD	–
SD1_TX2_N	SerDes Transmit Data (negative)	AE13	O	X1VDD	–
SD1_TX2_P	SerDes Transmit Data (positive)	AD13	O	X1VDD	–
SD1_TX3_N	SerDes Transmit Data (negative)	AE14	O	X1VDD	–
SD1_TX3_P	SerDes Transmit Data (positive)	AD14	O	X1VDD	–
SD1_TX4_N	SerDes Transmit Data (negative)	AE16	O	X1VDD	–
SD1_TX4_P	SerDes Transmit Data (positive)	AD16	O	X1VDD	–
SD1_TX5_N	SerDes Transmit Data (negative)	AE17	O	X1VDD	–
SD1_TX5_P	SerDes Transmit Data (positive)	AD17	O	X1VDD	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_TX6_N	SerDes Transmit Data (negative)	AE19	O	X1VDD	–
SD1_TX6_P	SerDes Transmit Data (positive)	AD19	O	X1VDD	–
SD1_TX7_N	SerDes Transmit Data (negative)	AE20	O	X1VDD	–
SD1_TX7_P	SerDes Transmit Data (positive)	AD20	O	X1VDD	–
USB PHY 1 & 2					
USB1_DRVVBUS	USB PHY Digital signal – Drive VBUS	F6	O	USB_HVDD	–
USB1_PWRFAULT	USB PHY Digital signal – Power Fault	F5	I	USB_HVDD	–
USB1_UDM	USB PHY Data Minus	F2	IO	USB_HVDD	–
USB1_UDP	USB PHY Data Plus	F1	IO	USB_HVDD	–
USB1_UID	USB PHY ID Detect	F4	I	USB_OVDD	–
USB1_VBUSCLMP	USB PHY VBUS	E4	I	USB_HVDD	–
USB2_DRVVBUS	USB PHY Digital signal – Drive VBUS	J5	O	USB_HVDD	–
USB2_PWRFAULT	USB PHY Digital signal – Power Fault	H5	I	USB_HVDD	–
USB2_UDM	USB PHY Data Minus	H2	IO	USB_HVDD	–
USB2_UDP	USB PHY Data Plus	H1	IO	USB_HVDD	–
USB2_UID	USB PHY ID Detect	H4	I	USB_OVDD	–
USB2_VBUSCLMP	USB PHY VBUS	J4	I	USB_HVDD	–
USB_IBIAS_REXT	USB PHY Impedance Calibration	G4	IO	USB_OVDD	(20)
IEEE1588					
TSEC_1588_ALARM_OUT1/ GPIO3_03	Alarm Out 1	AF5	O	LVDD	(1)
TSEC_1588_ALARM_OUT2/ GPIO3_04/EMI1_MDC	Alarm Out 2	AC7	O	LVDD	(1)
TSEC_1588_CLK_IN/ GPIO3_00	Clock In	AC8	I	LVDD	(1)
TSEC_1588_CLK_OUT/ GPIO3_05	Clock Out	AD7	O	LVDD	(1)
TSEC_1588_PULSE_OUT1/ GPIO3_06	Pulse Out 1	AE6	O	LVDD	(1)
TSEC_1588_PULSE_OUT2/ GPIO3_07	Pulse Out 2	AD8	O	LVDD	(1)
TSEC_1588_TRIG_IN1/ GPIO3_01	Trigger In 1	AB6	I	LVDD	(1)
TSEC_1588_TRIG_IN2/ GPIO3_02/EMI1_MDIO	Trigger In 2	AE5	I	LVDD	(1)
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	AH3	O	L1VDD	–
EMI1_MDC/**TSEC_1588_ALARM_OUT2**/ GPIO3_04	Management Data Clock	AC7	O	LVDD	(1)
EMI1_MDIO	Management Data In/Out	AH4	IO	L1VDD	–
EMI1_MDIO/ **TSEC_1588_TRIG_IN2**/ GPIO3_02	Management Data In/Out	AE5	IO	LVDD	–
Ethernet controller 1 and GPIO					
EC1_COL/GPIO3_10/ MII_COL/MAC2_MII_COL	Collison Detect	AC1	IO	L1VDD	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_GTX_CLK/GPIO3_16/ MII_TX_CLK/ MAC2_GTX_CLK/ MAC2_MII_TX_CLK	Transmit Clock Out	AF3	O	L1VDD	(1)
EC1_GTX_CLK125/ GPIO3_17/MII_CRS/ MAC2_GTX_CLK125/ MAC2_MII_CRS	Reference Clock	AG3	I	L1VDD	(1)
EC1_RXD0/GPIO3_21/ MII_RXD0/MAC2_RXD0/ MAC2_MII_RXD0	Receive Data	AF2	I	L1VDD	(1)
EC1_RXD1/GPIO3_20/ MII_RXD1/MAC2_RXD1/ MAC2_MII_RXD1	Receive Data	AF1	I	L1VDD	(1)
EC1_RXD2/GPIO3_19/ MII_RXD2/MAC2_RXD2/ MAC2_MII_RXD2	Receive Data	AE1	I	L1VDD	(1)
EC1_RXD3/GPIO3_18/ MII_RXD3/MAC2_RXD3/ MAC2_MII_RXD3	Receive Data	AD2	I	L1VDD	(1)
EC1_RX_CLK/GPIO3_23/ MII_RX_CLK/MAC2_RX_CLK/ MAC2_MII_RX_CLK	Receive Clock	AD1	I	L1VDD	(1)
EC1_RX_CTL/GPIO3_22/ MII_RX_DV/MAC2_RX_CTL/ MAC2_MII_RX_DV	Receive Data Valid	AG2	I	L1VDD	(1)
EC1_RX_ER/GPIO3_09/ MII_RX_ER/ MAC2_MII_RX_ER	Receive Error	AC2	IO	L1VDD	–
EC1_TXD0/GPIO3_14/ MII_TXD0/MAC2_TXD0/ MAC2_MII_TXD0	Transmit Data	AE3	O	L1VDD	(1)
EC1_TXD1/GPIO3_13/ MII_TXD1/MAC2_TXD1/ MAC2_MII_TXD1	Transmit Data	AE4	O	L1VDD	(1)
EC1_TXD2/GPIO3_12/ MII_TXD2/MAC2_TXD2/ MAC2_MII_TXD2	Transmit Data	AD3	O	L1VDD	(1)
EC1_TXD3/GPIO3_11/ MII_TXD3/MAC2_TXD3/ MAC2_MII_TXD3	Transmit Data	AC3	O	L1VDD	(1)
EC1_TX_CTL/GPIO3_15/ MII_TX_EN/MAC2_TX_CTL/ MAC2_MII_TX_EN	Transmit Enable	AF4	O	L1VDD	(1)(14)
EC1_TX_ER/GPIO3_08/ MII_TX_ER/ MAC2_MII_TX_ER	Transmit Error	AC4	IO	L1VDD	(14)
Ethernet controller 2 and GPIO					
EC2_GTX_CLK/GPIO4_28	Transmit Clock Out	AE8	O	LVDD	(1)
EC2_GTX_CLK125/GPIO4_29	Reference Clock	AC6	I	LVDD	(1)
EC2_RXD0/GPIO3_31	Receive Data	AH8	I	LVDD	(1)
EC2_RXD1/GPIO3_30	Receive Data	AG7	I	LVDD	(1)
EC2_RXD2/GPIO3_29	Receive Data	AH7	I	LVDD	(1)
EC2_RXD3/GPIO3_28	Receive Data	AH6	I	LVDD	(1)
EC2_RX_CLK/GPIO4_31	Receive Clock	AH5	I	LVDD	(1)
EC2_RX_CTL/GPIO4_30	Receive Data Valid	AG8	I	LVDD	(1)
EC2_TXD0/GPIO3_27	Transmit Data	AE7	O	LVDD	(1)
EC2_TXD1/GPIO3_26	Transmit Data	AF7	O	LVDD	(1)
EC2_TXD2/GPIO3_25	Transmit Data	AF6	O	LVDD	(1)
EC2_TXD3/GPIO3_24	Transmit Data	AG5	O	LVDD	(1)
EC2_TX_CTL/GPIO4_27	Transmit Enable	AF8	O	LVDD	(1)(14)

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DSYSCLK					
DIFF_SYSCLK	"Single Oscillator Source" Reference Clock Differential (positive)	G14	I	O1VDD	(18)
DIFF_SYSCLK_B	"Single Oscillator Source" Reference Clock Differential (negative)	F14	I	O1VDD	(18)
USB Clocking					
USBCLK	USB PHY Clock In	F8	I	O1VDD	(17)
I2C 3 & 4					
IIC3_SCL/GPIO4_00	Serial Clock	V2	IO	DVDD	(7)(8)
IIC3_SDA/GPIO4_01	Serial Data	W3	IO	DVDD	(7)(8)
IIC4_SCL/GPIO4_02/EVT5_B/ DIU_HSYNC	Serial Clock	AA3	IO	DVDD	(7)(8)
IIC4_SDA/GPIO4_03/EVT6_B/ DIU_VSYNC	Serial Data	AB3	IO	DVDD	(7)(8)
DMA					
DMA1_DACK0_B/GPIO4_05/ TDM_TFS	DMA1 channel 0 acknowledge	U5	O	DVDD	(1)
DMA1_DDONE0_B/ GPIO4_06/TDM_TCK	DMA1 channel 0 done	R5	O	DVDD	(1)
DMA1_DREQ0_B/GPIO4_04/ TDM_TXD	DMA1 channel 0 request	P5	I	DVDD	(1)
DMA2_DACK0_B/GPIO4_08/ EVT7_B/TDM_RFS	DMA2 channel 0 acknowledge	AA5	O	DVDD	(1)
DMA2_DDONE0_B/ GPIO4_09/EVT8_B/TDM_RCK	DMA2 channel 0 done	Y5	O	DVDD	(1)
DMA2_DREQ0_B/GPIO4_07/ TDM_RXD	DMA2 channel 0 request	V5	I	DVDD	(1)
QE_TDM					
CLK09/GPIO4_15/BRGO2/ DIU_D10	External Clock	P4	I	DVDD	(1)
CLK10/GPIO4_22/BRGO3/ DIU_D11	External Clock	P3	I	DVDD	(1)
CLK11/GPIO4_16/BRGO4/ DIU_DE	External Clock	N4	I	DVDD	(1)
CLK12/GPIO4_23/BRGO1/ DIU_CLK_OUT	External Clock	M4	I	DVDD	(1)(24)
TDMA_RQ/GPIO4_14/ UC1_CDB_RXER/DIU_D4	Request	R2	O	DVDD	(1)
TDMA_RSYNC/GPIO4_11/ UC1_CTSB_RXDV/DIU_D1	Receive Sync	U1	I	DVDD	(1)
TDMA_RXD/GPIO4_10/ UC1_RXD7/DIU_D0/ TDMA_TXD	Receive Data	U2	I	DVDD	(1)
TDMA_TSYNC/GPIO4_13/ UC1_RTSB_TXEN/DIU_D3	Transmit Sync	R1	I	DVDD	(1)
TDMA_TXD/GPIO4_12/ UC1_TXD7/DIU_D2/ TDMA_RXD_EXC	Transmit Data	T1	O	DVDD	(1)
TDMB_RQ/GPIO4_21/ UC3_CDB_RXER/DIU_D9	Request	R4	O	DVDD	(1)
TDMB_RSYNC/GPIO4_18/ UC3_CTSB_RXDV/DIU_D6	Receive Sync	T3	I	DVDD	(1)
TDMB_RXD/GPIO4_17/ UC3_RXD7/DIU_D5/ TDMB_TXD	Receive Data	U4	I	DVDD	(1)
TDMB_TSYNC/GPIO4_20/ UC3_RTSB_TXEN/DIU_D8	Transmit Sync	R3	I	DVDD	(1)
TDMB_TXD/GPIO4_19/ UC3_TXD7/DIU_D7/ TDMB_RXD_EXC	Transmit Data	T4	O	DVDD	(1)
eSDHC					

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CD_B/GPIO4_24	SDHC Card Detect	L5	I	CVDD	(1)
SDHC_CLK/GPIO2_09	Host to Card Clock	K1	IO	EVDD	–
SDHC_CLK_SYNC_IN/**IRQ10**/ GPIO1_30	Clock Sync	L4	I	CVDD	(1)
SDHC_CLK_SYNC_OUT/ **SPI_CS3_B**/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR	Clock Sync	N3	O	CVDD	(1)
SDHC_CMD/GPIO2_04	Command/Response	K3	IO	EVDD	–
SDHC_CMD_DIR/**SPI_CS1_B**/ GPIO2_01/SDHC_DAT5	CMD direction control	M2	O	CVDD	(1)
SDHC_DAT0/GPIO2_05	Data	L2	IO	EVDD	–
SDHC_DAT0_DIR/**SPI_CS2_B**/GPIO2_02/ SDHC_DAT6	Data	M3	O	CVDD	(1)
SDHC_DAT1/GPIO2_06	Data	K4	IO	EVDD	–
SDHC_DAT123_DIR/ **SPI_CS3_B**/GPIO2_03/ SDHC_DAT7/ SDHC_CLK_SYNC_OUT	Data	N3	O	CVDD	(1)
SDHC_DAT2/GPIO2_07	Data	L3	IO	EVDD	–
SDHC_DAT3/GPIO2_08	Data	L1	IO	EVDD	–
SDHC_DAT4/**SPI_CS0_B**/ GPIO2_00	Data	M1	IO	CVDD	–
SDHC_DAT5/**SPI_CS1_B**/ GPIO2_01/SDHC_CMD_DIR	Data	M2	IO	CVDD	–
SDHC_DAT6/**SPI_CS2_B**/ GPIO2_02/SDHC_DAT0_DIR	Data	M3	IO	CVDD	–
SDHC_DAT7/**SPI_CS3_B**/ GPIO2_03/ SDHC_DAT123_DIR/ SDHC_CLK_SYNC_OUT	Data	N3	IO	CVDD	–
SDHC_VS/**IRQ03**/GPIO1_23	Voltage Select	D1	IO	O1VDD	–
SDHC_WP/GPIO4_25	SDHC Write Protect	M5	I	CVDD	(1)
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**	Power-On-Reset Configuration Signal	C8	I	OVDD	(1)(4)
cfg_eng_use0/**IFC_WE0_B**	Power-On-Reset Configuration Signal	D13	I	OVDD	(1)
cfg_eng_use1/**IFC_OE_B**	Power-On-Reset Configuration Signal	D15	I	OVDD	(1)(21)
cfg_eng_use2/**IFC_WP0_B**	Power-On-Reset Configuration Signal	F17	I	OVDD	(1)
cfg_gpinput0/**IFC_AD00**	Power-On-Reset Configuration Signal	A4	I	OVDD	(1)(4)
cfg_gpinput1/**IFC_AD01**	Power-On-Reset Configuration Signal	B5	I	OVDD	(1)(4)
cfg_gpinput2/**IFC_AD02**	Power-On-Reset Configuration Signal	A5	I	OVDD	(1)(4)
cfg_gpinput3/**IFC_AD03**	Power-On-Reset Configuration Signal	B6	I	OVDD	(1)(4)
cfg_gpinput4/**IFC_AD04**	Power-On-Reset Configuration Signal	A6	I	OVDD	(1)(4)
cfg_gpinput5/**IFC_AD05**	Power-On-Reset Configuration Signal	A7	I	OVDD	(1)(4)
cfg_gpinput6/**IFC_AD06**	Power-On-Reset Configuration Signal	B8	I	OVDD	(1)(4)
cfg_gpinput7/**IFC_AD07**	Power-On-Reset Configuration Signal	A8	I	OVDD	(1)(4)
cfg_ifc_te/**IFC_TE**	Power-On-Reset Configuration Signal	B14	I	OVDD	(1)(4)
cfg_rcw_src0/**IFC_AD08**	Power-On-Reset Configuration Signal	B9	I	OVDD	(1)(4)
cfg_rcw_src1/**IFC_AD09**	Power-On-Reset Configuration Signal	A9	I	OVDD	(1)(4)
cfg_rcw_src2/**IFC_AD10**	Power-On-Reset Configuration Signal	A10	I	OVDD	(1)(4)

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_rcw_src3/**IFC_AD11**	Power-On-Reset Configuration Signal	B11	I	OV_{DD}	(1)(4)
cfg_rcw_src4/**IFC_AD12**	Power-On-Reset Configuration Signal	A11	I	OV_{DD}	(1)(4)
cfg_rcw_src5/**IFC_AD13**	Power-On-Reset Configuration Signal	B12	I	OV_{DD}	(1)(4)
cfg_rcw_src6/**IFC_AD14**	Power-On-Reset Configuration Signal	A12	I	OV_{DD}	(1)(4)
cfg_rcw_src7/**IFC_AD15**	Power-On-Reset Configuration Signal	A13	I	OV_{DD}	(1)(4)
cfg_rcw_src8/**IFC_CLE**	Power-On-Reset Configuration Signal	F16	I	OV_{DD}	(1)(4)
General Purpose Input/Output					
GPIO1_09/**IFC_CS4_B**	General Purpose Input/Output	E17	IO	OV_{DD}	–
GPIO1_10/**IFC_CS5_B**	General Purpose Input/Output	C17	IO	OV_{DD}	–
GPIO1_11/**IFC_CS6_B**	General Purpose Input/Output	D18	IO	OV_{DD}	–
GPIO1_12/**IFC_CS7_B**	General Purpose Input/Output	C19	IO	OV_{DD}	–
GPO1_13/**ASLEEP**	General Purpose Input/Output	B2	O	$O1V_{DD}$	(1)
GPIO1_14/**RTC**	General Purpose Input/Output	B17	IO	OV_{DD}	–
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	AA2	IO	DV_{DD}	–
GPIO1_16/**UART2_SOUT**	General Purpose Input/Output	AA4	IO	DV_{DD}	–
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	AA1	IO	DV_{DD}	–
GPIO1_18/**UART2_SIN**	General Purpose Input/Output	W4	IO	DV_{DD}	–
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT	General Purpose Input/Output	Y1	IO	DV_{DD}	–
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT	General Purpose Input/Output	V4	IO	DV_{DD}	–
GPIO1_21/**UART1_CTS_B**/ UART3_SIN	General Purpose Input/Output	Y2	IO	DV_{DD}	–
GPIO1_22/**UART2_CTS_B**/ UART4_SIN	General Purpose Input/Output	Y4	IO	DV_{DD}	–
GPIO1_23/**IRQ03**/SDHC_VS	General Purpose Input/Output	D1	IO	$O1V_{DD}$	–
GPIO1_24/**IRQ04**	General Purpose Input/Output	D4	IO	$O1V_{DD}$	–
GPIO1_25/**IRQ05**	General Purpose Input/Output	D5	IO	$O1V_{DD}$	–
GPIO1_26/**IRQ06**	General Purpose Input/Output	AB4	IO	$L1V_{DD}$	–
GPIO1_27/**IRQ07**	General Purpose Input/Output	AD5	IO	$L1V_{DD}$	–
GPIO1_28/**IRQ08**	General Purpose Input/Output	AB1	IO	$L1V_{DD}$	–
GPIO1_29/**IRQ09**	General Purpose Input/Output	AC5	IO	$L1V_{DD}$	–
GPIO1_30/**IRQ10**/ SDHC_CLK_SYNC_IN	General Purpose Input/Output	L4	IO	CV_{DD}	–
GPIO1_31/**IRQ11**	General Purpose Input/Output	U3	IO	DV_{DD}	–
GPIO2_00/**SPI_CS0_B**/ SDHC_DAT4	General Purpose Input/Output	M1	IO	CV_{DD}	–
GPIO2_01/**SPI_CS1_B**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	M2	IO	CV_{DD}	–
GPIO2_02/**SPI_CS2_B**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	M3	IO	CV_{DD}	–
GPIO2_03/**SPI_CS3_B**/ SDHC_DAT7/ SDHC_DAT123_DIR/ SDHC_CLK_SYNC_OUT	General Purpose Input/Output	N3	IO	CV_{DD}	–
GPIO2_04/**SDHC_CMD**	General Purpose Input/Output	K3	IO	EV_{DD}	–
GPIO2_05/**SDHC_DAT0**	General Purpose Input/Output	L2	IO	EV_{DD}	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_06/**SDHC_DAT1**	General Purpose Input/Output	K4	IO	EV_{DD}	–
GPIO2_07/**SDHC_DAT2**	General Purpose Input/Output	L3	IO	EV_{DD}	–
GPIO2_08/**SDHC_DAT3**	General Purpose Input/Output	L1	IO	EV_{DD}	–
GPIO2_09/**SDHC_CLK**	General Purpose Input/Output	K1	IO	EV_{DD}	–
GPIO2_10/**IFC_CS1_B**	General Purpose Input/Output	E15	IO	OV_{DD}	–
GPIO2_11/**IFC_CS2_B**	General Purpose Input/Output	D16	IO	OV_{DD}	–
GPIO2_12/**IFC_CS3_B**	General Purpose Input/Output	C16	IO	OV_{DD}	–
GPIO2_13/**IFC_PAR0**	General Purpose Input/Output	C15	IO	OV_{DD}	–
GPIO2_14/**IFC_PAR1**	General Purpose Input/Output	C14	IO	OV_{DD}	–
GPIO2_15/**IFC_PERR_B**	General Purpose Input/Output	E14	IO	OV_{DD}	–
GPIO2_25/**IFC_A25**/ IFC_WP1_B	General Purpose Input/Output	C10	IO	OV_{DD}	–
GPIO2_26/**IFC_A26**/ IFC_WP2_B	General Purpose Input/Output	E11	IO	OV_{DD}	–
GPIO2_27/**IFC_A27**/ IFC_WP3_B	General Purpose Input/Output	C11	IO	OV_{DD}	–
GPIO2_28/**IFC_A28**	General Purpose Input/Output	D11	IO	OV_{DD}	–
GPIO2_29/**IFC_A29**/ IFC_RB2_B	General Purpose Input/Output	C12	IO	OV_{DD}	–
GPIO2_30/**IFC_A30**/ IFC_RB3_B	General Purpose Input/Output	D12	IO	OV_{DD}	–
GPIO2_31/**IFC_A31**/ IFC_RB4_B	General Purpose Input/Output	E12	IO	OV_{DD}	–
GPIO3_00/ TSEC_1588_CLK_IN	General Purpose Input/Output	AC8	IO	LV_{DD}	–
GPIO3_01/ TSEC_1588_TRIG_IN1	General Purpose Input/Output	AB6	IO	LV_{DD}	–
GPIO3_02/ **TSEC_1588_TRIG_IN2**/ EMI1_MDIO	General Purpose Input/Output	AE5	IO	LV_{DD}	–
GPIO3_03/ TSEC_1588_ALARM_OUT1	General Purpose Input/Output	AF5	IO	LV_{DD}	–
GPIO3_04/ **TSEC_1588_ALARM_OUT2**/ EMI1_MDC	General Purpose Input/Output	AC7	IO	LV_{DD}	–
GPIO3_05/ TSEC_1588_CLK_OUT	General Purpose Input/Output	AD7	IO	LV_{DD}	–
GPIO3_06/ TSEC_1588_PULSE_OUT1	General Purpose Input/Output	AE6	IO	LV_{DD}	–
GPIO3_07/ TSEC_1588_PULSE_OUT2	General Purpose Input/Output	AD8	IO	LV_{DD}	–
GPIO3_08/**EC1_TX_ER**/ MII_TX_ER/ MAC2_MII_TX_ER	General Purpose Input/Output	AC4	IO	$L1V_{DD}$	–
GPIO3_09/**EC1_RX_ER**/ MII_RX_ER/ MAC2_MII_RX_ER	General Purpose Input/Output	AC2	IO	$L1V_{DD}$	–
GPIO3_10/**EC1_COL**/ MII_COL/MAC2_MII_COL	General Purpose Input/Output	AC1	IO	$L1V_{DD}$	–
GPIO3_11/**EC1_TXD3**/ MII_TXD3/MAC2_TXD3/ MAC2_MII_TXD3	General Purpose Input/Output	AC3	IO	$L1V_{DD}$	–
GPIO3_12/**EC1_TXD2**/ MII_TXD2/MAC2_TXD2/ MAC2_MII_TXD2	General Purpose Input/Output	AD3	IO	$L1V_{DD}$	–
GPIO3_13/**EC1_TXD1**/ MII_TXD1/MAC2_TXD1/ MAC2_MII_TXD1	General Purpose Input/Output	AE4	IO	$L1V_{DD}$	–
GPIO3_14/**EC1_TXD0**/ MII_TXD0/MAC2_TXD0/ MAC2_MII_TXD0	General Purpose Input/Output	AE3	IO	$L1V_{DD}$	–
GPIO3_15/**EC1_TX_CTL**/ MII_TX_EN/MAC2_TX_CTL/ MAC2_MII_TX_EN	General Purpose Input/Output	AF4	IO	$L1V_{DD}$	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_16/**EC1_GTX_CLK**/ MII_TX_CLK/ MAC2_GTX_CLK/ MAC2_MII_TX_CLK	General Purpose Input/Output	AF3	IO	L1V_{DD}	–
GPIO3_17/ **EC1_GTX_CLK125**/MII_CRS/ MAC2_GTX_CLK125/ MAC2_MII_CRS	General Purpose Input/Output	AG3	IO	L1V_{DD}	–
GPIO3_18/**EC1_RXD3**/ MII_RXD3/MAC2_RXD3/ MAC2_MII_RXD3	General Purpose Input/Output	AD2	IO	L1V_{DD}	–
GPIO3_19/**EC1_RXD2**/ MII_RXD2/MAC2_RXD2/ MAC2_MII_RXD2	General Purpose Input/Output	AE1	IO	L1V_{DD}	–
GPIO3_20/**EC1_RXD1**/ MII_RXD1/MAC2_RXD1/ MAC2_MII_RXD1	General Purpose Input/Output	AF1	IO	L1V_{DD}	–
GPIO3_21/**EC1_RXD0**/ MII_RXD0/MAC2_RXD0/ MAC2_MII_RXD0	General Purpose Input/Output	AF2	IO	L1V_{DD}	–
GPIO3_22/**EC1_RX_CTL**/ MII_RX_DV/MAC2_RX_CTL/ MAC2_MII_RX_DV	General Purpose Input/Output	AG2	IO	L1V_{DD}	–
GPIO3_23/**EC1_RX_CLK**/ MII_RX_CLK/MAC2_RX_CLK/ MAC2_MII_RX_CLK	General Purpose Input/Output	AD1	IO	L1V_{DD}	–
GPIO3_24/**EC2_TXD3**	General Purpose Input/Output	AG5	IO	LV_{DD}	–
GPIO3_25/**EC2_TXD2**	General Purpose Input/Output	AF6	IO	LV_{DD}	–
GPIO3_26/**EC2_TXD1**	General Purpose Input/Output	AF7	IO	LV_{DD}	–
GPIO3_27/**EC2_TXD0**	General Purpose Input/Output	AE7	IO	LV_{DD}	–
GPIO3_28/**EC2_RXD3**	General Purpose Input/Output	AH6	IO	LV_{DD}	–
GPIO3_29/**EC2_RXD2**	General Purpose Input/Output	AH7	IO	LV_{DD}	–
GPIO3_30/**EC2_RXD1**	General Purpose Input/Output	AG7	IO	LV_{DD}	–
GPIO3_31/**EC2_RXD0**	General Purpose Input/Output	AH8	IO	LV_{DD}	–
GPIO4_00/**IIC3_SCL**	General Purpose Input/Output	V2	IO	DV$_{DD}$	–
GPIO4_01/**IIC3_SDA**	General Purpose Input/Output	W3	IO	DV$_{DD}$	–
GPIO4_02/**IIC4_SCL**/EVT5_B/ DIU_HSYNC	General Purpose Input/Output	AA3	IO	DV$_{DD}$	–
GPIO4_03/**IIC4_SDA**/EVT6_B/ DIU_VSYNC	General Purpose Input/Output	AB3	IO	DV$_{DD}$	–
GPIO4_04/**DMA1_DREQ0_B**/ TDM_TXD	General Purpose Input/Output	P5	IO	DV$_{DD}$	–
GPIO4_05/**DMA1_DACK0_B**/ TDM_TFS	General Purpose Input/Output	U5	IO	DV$_{DD}$	–
GPIO4_06/**DMA1_DDONE0_B**/TDM_TCK	General Purpose Input/Output	R5	IO	DV$_{DD}$	–
GPIO4_07/**DMA2_DREQ0_B**/ TDM_RXD	General Purpose Input/Output	V5	IO	DV$_{DD}$	–
GPIO4_08/**DMA2_DACK0_B**/ EVT7_B/TDM_RFS	General Purpose Input/Output	AA5	IO	DV$_{DD}$	–
GPIO4_09/**DMA2_DDONE0_B**/EVT8_B/ TDM_RCK	General Purpose Input/Output	Y5	IO	DV$_{DD}$	–
GPIO4_10/**TDMA_RXD**/ UC1_RXD7/DIU_D0	General Purpose Input/Output	U2	IO	DV$_{DD}$	–
GPIO4_11/**TDMA_RSYNC**/ UC1_CTSB_RXDV/DIU_D1	General Purpose Input/Output	U1	IO	DV$_{DD}$	–
GPIO4_12/**TDMA_TXD**/ UC1_TXD7/DIU_D2	General Purpose Input/Output	T1	IO	DV$_{DD}$	–
GPIO4_13/**TDMA_TSYNC**/ UC1_RTSB_TXEN/DIU_D3	General Purpose Input/Output	R1	IO	DV$_{DD}$	–
GPIO4_14/**TDMA_RQ**/ UC1_CDB_RXER/DIU_D4	General Purpose Input/Output	R2	IO	DV$_{DD}$	–
GPIO4_15/**CLK09**/BRGO2/ DIU_D10	General Purpose Input/Output	P4	IO	DV$_{DD}$	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO4_16/**CLK11**/BRGO4/ DIU_DE	General Purpose Input/Output	N4	IO	DV_{DD}	–
GPIO4_17/**TDMB_RXD**/ UC3_RXD7/DIU_D5	General Purpose Input/Output	U4	IO	DV_{DD}	–
GPIO4_18/**TDMB_RSYNC**/ UC3_CTSB_RXDV/DIU_D6	General Purpose Input/Output	T3	IO	DV_{DD}	–
GPIO4_19/**TDMB_TXD**/ UC3_TXD7/DIU_D7	General Purpose Input/Output	T4	IO	DV_{DD}	–
GPIO4_20/**TDMB_TSYNC**/ UC3_RTSB_TXEN/DIU_D8	General Purpose Input/Output	R3	IO	DV_{DD}	–
GPIO4_21/**TDMB_RQ**/ UC3_CDB_RXER/DIU_D9	General Purpose Input/Output	R4	IO	DV_{DD}	–
GPIO4_22/**CLK10**/BRGO3/ DIU_D11	General Purpose Input/Output	P3	IO	DV_{DD}	–
GPIO4_23/**CLK12**/BRGO1/ DIU_CLK_OUT	General Purpose Input/Output	M4	IO	DV_{DD}	–
GPIO4_24/**SDHC_CD_B**	General Purpose Input/Output	L5	IO	CV_{DD}	–
GPIO4_25/**SDHC_WP**	General Purpose Input/Output	M5	IO	CV_{DD}	–
GPIO4_27/**EC2_TX_CTL**	General Purpose Input/Output	AF8	IO	LV_{DD}	–
GPIO4_28/**EC2_GTX_CLK**	General Purpose Input/Output	AE8	IO	LV_{DD}	–
GPIO4_29/**EC2_GTX_CLK125**	General Purpose Input/Output	AC6	IO	LV_{DD}	–
GPIO4_30/**EC2_RX_CTL**	General Purpose Input/Output	AG8	IO	LV_{DD}	–
GPIO4_31/**EC2_RX_CLK**	General Purpose Input/Output	AH5	IO	LV_{DD}	–
DIU					
DIU_CLK_OUT/**CLK12**/ GPIO4_23/BRGO1	Pixel Clock	M4	O	DV_{DD}	(1)
DIU_D0/**TDMA_RXD**/ GPIO4_10/UC1_RXD7	DIU Data	U2	O	DV_{DD}	(1)
DIU_D1/**TDMA_RSYNC**/ GPIO4_11/UC1_CTSB_RXDV	DIU Data	U1	O	DV_{DD}	(1)
DIU_D10/**CLK09**/GPIO4_15/ BRGO2	DIU Data	P4	O	DV_{DD}	(1)
DIU_D11/**CLK10**/GPIO4_22/ BRGO3	DIU Data	P3	O	DV_{DD}	(1)
DIU_D2/**TDMA_TXD**/ GPIO4_12/UC1_TXD7	DIU Data	T1	O	DV_{DD}	(1)
DIU_D3/**TDMA_TSYNC**/ GPIO4_13/UC1_RTSB_TXEN	DIU Data	R1	O	DV_{DD}	(1)
DIU_D4/**TDMA_RQ**/ GPIO4_14/UC1_CDB_RXER	DIU Data	R2	O	DV_{DD}	(1)
DIU_D5/**TDMB_RXD**/ GPIO4_17/UC3_RXD7	DIU Data	U4	O	DV_{DD}	(1)
DIU_D6/**TDMB_RSYNC**/ GPIO4_18/UC3_CTSB_RXDV	DIU Data	T3	O	DV_{DD}	(1)
DIU_D7/**TDMB_TXD**/ GPIO4_19/UC3_TXD7	DIU Data	T4	O	DV_{DD}	(1)
DIU_D8/**TDMB_TSYNC**/ GPIO4_20/UC3_RTSB_TXEN	DIU Data	R3	O	DV_{DD}	(1)
DIU_D9/**TDMB_RQ**/ GPIO4_21/UC3_CDB_RXER	DIU Data	R4	O	DV_{DD}	(1)
DIU_DE/**CLK11**/GPIO4_16/ BRGO4	Data Enable	N4	O	DV_{DD}	(1)
DIU_HSYNC/**IIC4_SCL**/ GPIO4_02/EVT5_B	Horizontal sync	AA3	O	DV_{DD}	(1)
DIU_VSYNC/**IIC4_SDA**/ GPIO4_03/EVT6_B	Vertical sync	AB3	O	DV_{DD}	(1)
TDM					
TDM_RCK/ **DMA2_DDONE0_B**/ GPIO4_09/EVT8_B	Receive clock	Y5	IO	DV_{DD}	–
TDM_RFS/**DMA2_DACK0_B**/ GPIO4_08/EVT7_B	Receive frame sync	AA5	IO	DV_{DD}	–
TDM_RXD/**DMA2_DREQ0_B**/ GPIO4_07	Receive data	V5	I	DV_{DD}	(1)
TDM_TCK/**DMA1_DDONE0_B**/GPIO4_06	Transmit clock	R5	IO	DV_{DD}	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TDM_TFS/**DMA1_DACK0_B**/ GPIO4_05	Transmit frame sync	U5	IO	DV_{DD}	–
TDM_TXD/**DMA1_DREQ0_B**/ GPIO4_04	Transmit data	P5	O	DV_{DD}	(1)
QE					
BRGO1/**CLK12**/GPIO4_23/ DIU_CLK_OUT	Baud rate generator	M4	O	DV_{DD}	(1)
BRGO2/**CLK09**/GPIO4_15/ DIU_D10	Baud rate generator	P4	O	DV_{DD}	(1)
BRGO3/**CLK10**/GPIO4_22/ DIU_D11	Baud rate generator	P3	O	DV_{DD}	(1)
BRGO4/**CLK11**/GPIO4_16/ DIU_DE	Baud rate generator	N4	O	DV_{DD}	(1)
UC1_CDB_RXER/**TDMA_RQ**/ GPIO4_14/DIU_D4	Receive Error	R2	I	DV_{DD}	(1)
UC1_CTSB_RXDV/**TDMA_RSYNC**/GPIO4_11/ DIU_D1	Receive DV	U1	I	DV_{DD}	(1)
UC1_RTSB_TXEN/**TDMA_TSYNC**/GPIO4_13/ DIU_D3	Transmit Enable	R1	O	DV_{DD}	(1)
UC1_RXD7/**TDMA_RXD**/ GPIO4_10/DIU_D0	Receive Data	U2	I	DV_{DD}	(1)
UC1_TXD7/**TDMA_TXD**/ GPIO4_12/DIU_D2	Transmit Data	T1	O	DV_{DD}	(1)
UC3_CDB_RXER/**TDMB_RQ**/ GPIO4_21/DIU_D9	Receive Error	R4	I	DV_{DD}	(1)
UC3_CTSB_RXDV/ **TDMB_RSYNC**/GPIO4_18/ DIU_D6	Receive DV	T3	I	DV_{DD}	(1)
UC3_RTSB_TXEN/**TDMB_TSYNC**/GPIO4_20/ DIU_D8	Transmit Enable	R3	O	DV_{DD}	(1)
UC3_RXD7/**TDMB_RXD**/ GPIO4_17/DIU_D5	Receive Data	U4	I	DV_{DD}	(1)
UC3_TXD7/**TDMB_TXD**/ GPIO4_19/DIU_D7	Transmit Data	T4	O	DV_{DD}	(1)
Power and Ground Signals					
GND	GND	F10			
GND	GND	G6			
GND	GND	H6			
GND	GND	J6			
GND	GND	J20			
GND	GND	A2			
GND	GND	A20			
GND	GND	A21			
GND	GND	A23			
GND	GND	A25			
GND	GND	A27			
GND	GND	A29			
GND	GND	A31			
GND	GND	A33			
GND	GND	A35			
GND	GND	A37			
GND	GND	A39			
GND	GND	A41			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	A43			
GND	GND	B1			
GND	GND	B4			
GND	GND	B7			
GND	GND	B10			
GND	GND	B13			
GND	GND	B16			
GND	GND	B19			
GND	GND	B22			
GND	GND	B24			
GND	GND	B26			
GND	GND	B28			
GND	GND	B30			
GND	GND	B32			
GND	GND	B34			
GND	GND	B36			
GND	GND	B38			
GND	GND	B40			
GND	GND	B42			
GND	GND	B44			
GND	GND	C21			
GND	GND	C23			
GND	GND	C25			
GND	GND	C27			
GND	GND	C29			
GND	GND	C31			
GND	GND	C33			
GND	GND	C35			
GND	GND	C37			
GND	GND	C39			
GND	GND	C41			
GND	GND	C43			
GND	GND	D2			
GND	GND	D20			
GND	GND	D21			
GND	GND	D22			
GND	GND	D24			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	D26			
GND	GND	D28			
GND	GND	E5			
GND	GND	E7			
GND	GND	E10			
GND	GND	E13			
GND	GND	E16			
GND	GND	E19			
GND	GND	E23			
GND	GND	E25			
GND	GND	E27			
GND	GND	F15			
GND	GND	F22			
GND	GND	F24			
GND	GND	F26			
GND	GND	G7			
GND	GND	G13			
GND	GND	G16			
GND	GND	G23			
GND	GND	G25			
GND	GND	G27			
GND	GND	H7			
GND	GND	H8			
GND	GND	H9			
GND	GND	H10			
GND	GND	H11			
GND	GND	H12			
GND	GND	H13			
GND	GND	H14			
GND	GND	H15			
GND	GND	H16			
GND	GND	H17			
GND	GND	H18			
GND	GND	H19			
GND	GND	H20			
GND	GND	H22			
GND	GND	H24			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	H26			
GND	GND	H28			
GND	GND	J7			
GND	GND	J23			
GND	GND	J25			
GND	GND	J27			
GND	GND	K2			
GND	GND	K5			
GND	GND	K6			
GND	GND	K7			
GND	GND	K12			
GND	GND	K14			
GND	GND	K16			
GND	GND	K18			
GND	GND	K20			
GND	GND	K22			
GND	GND	K24			
GND	GND	K26			
GND	GND	K28			
GND	GND	L7			
GND	GND	L9			
GND	GND	L11			
GND	GND	L13			
GND	GND	L15			
GND	GND	L17			
GND	GND	L19			
GND	GND	L23			
GND	GND	L25			
GND	GND	L27			
GND	GND	M7			
GND	GND	M10			
GND	GND	M12			
GND	GND	M14			
GND	GND	M16			
GND	GND	M18			
GND	GND	M20			
GND	GND	M22			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	M24			
GND	GND	M26			
GND	GND	M28			
GND	GND	N2			
GND	GND	N5			
GND	GND	N7			
GND	GND	N9			
GND	GND	N11			
GND	GND	N13			
GND	GND	N15			
GND	GND	N17			
GND	GND	N19			
GND	GND	N23			
GND	GND	N25			
GND	GND	N27			
GND	GND	P7			
GND	GND	P10			
GND	GND	P12			
GND	GND	P14			
GND	GND	P16			
GND	GND	P18			
GND	GND	P20			
GND	GND	P22			
GND	GND	P24			
GND	GND	P26			
GND	GND	P28			
GND	GND	R7			
GND	GND	R9			
GND	GND	R11			
GND	GND	R13			
GND	GND	R15			
GND	GND	R17			
GND	GND	R19			
GND	GND	R23			
GND	GND	R25			
GND	GND	R27			
GND	GND	T2			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	T5			
GND	GND	T7			
GND	GND	T10			
GND	GND	T12			
GND	GND	T14			
GND	GND	T16			
GND	GND	T18			
GND	GND	T20			
GND	GND	T22			
GND	GND	T24			
GND	GND	T26			
GND	GND	T28			
GND	GND	U7			
GND	GND	U9			
GND	GND	U11			
GND	GND	U13			
GND	GND	U15			
GND	GND	U17			
GND	GND	U19			
GND	GND	U23			
GND	GND	U25			
GND	GND	V7			
GND	GND	V10			
GND	GND	V12			
GND	GND	V14			
GND	GND	V16			
GND	GND	V18			
GND	GND	V20			
GND	GND	V22			
GND	GND	V24			
GND	GND	V26			
GND	GND	W2			
GND	GND	W5			
GND	GND	W7			
GND	GND	W9			
GND	GND	W11			
GND	GND	W13			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	W23			
GND	GND	W25			
GND	GND	Y7			
GND	GND	Y10			
GND	GND	Y12			
GND	GND	Y22			
GND	GND	Y24			
GND	GND	Y26			
GND	GND	AA11			
GND	GND	AA23			
GND	GND	AA25			
GND	GND	AB2			
GND	GND	AB5			
GND	GND	AB7			
GND	GND	AB22			
GND	GND	AB24			
GND	GND	AB26			
GND	GND	AB28			
GND	GND	AC23			
GND	GND	AC25			
GND	GND	AC27			
GND	GND	AD4			
GND	GND	AD6			
GND	GND	AD22			
GND	GND	AD24			
GND	GND	AD26			
GND	GND	AD28			
GND	GND	AE2			
GND	GND	AE23			
GND	GND	AE25			
GND	GND	AE27			
GND	GND	AF9			
GND	GND	AF21			
GND	GND	AF22			
GND	GND	AF24			
GND	GND	AF26			
GND	GND	AF28			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	AF30			
GND	GND	AF32			
GND	GND	AF34			
GND	GND	AF36			
GND	GND	AF38			
GND	GND	AF40			
GND	GND	AF42			
GND	GND	AF44			
GND	GND	AG1			
GND	GND	AG4			
GND	GND	AG6			
GND	GND	AG23			
GND	GND	AG25			
GND	GND	AG27			
GND	GND	AG29			
GND	GND	AG31			
GND	GND	AG33			
GND	GND	AG35			
GND	GND	AG37			
GND	GND	AG39			
GND	GND	AG41			
GND	GND	AG43			
GND	GND	AH2			
GND	GND	AH22			
GND	GND	AH24			
GND	GND	AH26			
GND	GND	AH28			
GND	GND	AH30			
GND	GND	AH32			
GND	GND	AH34			
GND	GND	AH36			
GND	GND	AH38			
GND	GND	AH40			
GND	GND	AH42			
GND	GND	AH44			
GND	GND	G17			
GND	GND	M9			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	GND	N6			
GND	GND	P9			
GND	GND	T6			
GND	GND	T9			
GND	GND	U6			
GND	GND	V6			
GND	GND	V9			
GND	GND	W6			
GND	GND	Y6			
GND	GND	Y8			
GND	GND	Y9			
GND	GND	Y11			
GND	GND	AA6			
GND	GND	AA7			
GND	GND	AA8			
GND	GND	AA9			
GND	GND	AA10			
GND	GND	AB8			
GND	GND	AB11			
GND	GND	AB12			
GND	GND	F11			
GND	GND	G18			
USB_AGND01	USB PHY Transceiver GND	E1	–	–	–
USB_AGND02	USB PHY Transceiver GND	E2	–	–	–
USB_AGND03	USB PHY Transceiver GND	E3	–	–	–
USB_AGND04	USB PHY Transceiver GND	F3	–	–	–
USB_AGND05	USB PHY Transceiver GND	G1	–	–	–
USB_AGND06	USB PHY Transceiver GND	G2	–	–	–
USB_AGND07	USB PHY Transceiver GND	G3	–	–	–
USB_AGND08	USB PHY Transceiver GND	G5	–	–	–
USB_AGND09	USB PHY Transceiver GND	H3	–	–	–
USB_AGND10	USB PHY Transceiver GND	J1	–	–	–
USB_AGND11	USB PHY Transceiver GND	J2	–	–	–
USB_AGND12	USB PHY Transceiver GND	J3	–	–	–
X1GND01	Serdes 1 transceiver GND	AC10	–	–	–
X1GND02	Serdes 1 transceiver GND	AC11	–	–	–
X1GND03	Serdes 1 transceiver GND	AC13	–	–	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X1GND04	Serdes 1 transceiver GND	AC14	–	–	–
X1GND05	Serdes 1 transceiver GND	AC16	–	–	–
X1GND06	Serdes 1 transceiver GND	AC17	–	–	–
X1GND07	Serdes 1 transceiver GND	AC19	–	–	–
X1GND08	Serdes 1 transceiver GND	AC20	–	–	–
X1GND09	Serdes 1 transceiver GND	AD9	–	–	–
X1GND10	Serdes 1 transceiver GND	AD12	–	–	–
X1GND11	Serdes 1 transceiver GND	AD15	–	–	–
X1GND12	Serdes 1 transceiver GND	AD18	–	–	–
X1GND13	Serdes 1 transceiver GND	AD21	–	–	–
X1GND14	Serdes 1 transceiver GND	AE9	–	–	–
X1GND15	Serdes 1 transceiver GND	AE12	–	–	–
X1GND16	Serdes 1 transceiver GND	AE15	–	–	–
X1GND17	Serdes 1 transceiver GND	AE18	–	–	–
X1GND18	Serdes 1 transceiver GND	AE21	–	–	–
S1GND01	Serdes 1 core logic GND	Y14	–	–	–
S1GND02	Serdes 1 core logic GND	Y16	–	–	–
S1GND03	Serdes 1 core logic GND	Y17	–	–	–
S1GND04	Serdes 1 core logic GND	Y18	–	–	–
S1GND05	Serdes 1 core logic GND	AA13	–	–	–
S1GND06	Serdes 1 core logic GND	AA15	–	–	–
S1GND07	Serdes 1 core logic GND	AA17	–	–	–
S1GND08	Serdes 1 core logic GND	AA19	–	–	–
S1GND09	Serdes 1 core logic GND	AA21	–	–	–
S1GND10	Serdes 1 core logic GND	AB13	–	–	–
S1GND11	Serdes 1 core logic GND	AB17	–	–	–
S1GND12	Serdes 1 core logic GND	AB21	–	–	–
S1GND13	Serdes 1 core logic GND	AF10	–	–	–
S1GND14	Serdes 1 core logic GND	AF11	–	–	–
S1GND15	Serdes 1 core logic GND	AF12	–	–	–
S1GND16	Serdes 1 core logic GND	AF13	–	–	–
S1GND17	Serdes 1 core logic GND	AF14	–	–	–
S1GND18	Serdes 1 core logic GND	AF15	–	–	–
S1GND19	Serdes 1 core logic GND	AF16	–	–	–
S1GND20	Serdes 1 core logic GND	AF17	–	–	–
S1GND21	Serdes 1 core logic GND	AF18	–	–	–
S1GND22	Serdes 1 core logic GND	AF19	–	–	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S1GND23	Serdes 1 core logic GND	AF20	–	–	–
S1GND24	Serdes 1 core logic GND	AG9	–	–	–
S1GND25	Serdes 1 core logic GND	AG12	–	–	–
S1GND26	Serdes 1 core logic GND	AG15	–	–	–
S1GND27	Serdes 1 core logic GND	AG18	–	–	–
S1GND28	Serdes 1 core logic GND	AG21	–	–	–
S1GND29	Serdes 1 core logic GND	AH9	–	–	–
S1GND30	Serdes 1 core logic GND	AH12	–	–	–
S1GND31	Serdes 1 core logic GND	AH15	–	–	–
S1GND32	Serdes 1 core logic GND	AH18	–	–	–
S1GND33	Serdes 1 core logic GND	AH21	–	–	–
AGND_SD1_PLL1	Serdes 1 PLL 1 GND	AA16	–	–	–
AGND_SD1_PLL2	Serdes 1 PLL 2 GND	AA20	–	–	–
SENSEGND	GND Sense pin	G20	–	–	–
SENSEGNDC	GND Sense pin for VDDC domain	AB10	–	–	–
O1VDD1	General I/O supply – Always on	J11	–	$O1V_{DD}$	–
O1VDD2	General I/O supply – Always on	J12	–	$O1V_{DD}$	–
O1VDD3	General I/O supply – Always on	J13	–	$O1V_{DD}$	–
OVDD1	General I/O supply – Switchable	J14	–	OV_{DD}	–
OVDD2	General I/O supply – Switchable	J15	–	OV_{DD}	–
OVDD3	General I/O supply – Switchable	J16	–	OV_{DD}	–
OVDD4	General I/O supply – Switchable	J17	–	OV_{DD}	–
OVDD5	General I/O supply – Switchable	J18	–	OV_{DD}	–
OVDD6	General I/O supply – Switchable	J19	–	OV_{DD}	–
DVDD1	UART/I2C/DMA/TDM supply – Switchable	N8	–	DV_{DD}	–
DVDD2	UART/I2C/DMA/TDM supply – Switchable	P8	–	DV_{DD}	–
DVDD3	UART/I2C/DMA/TDM supply – Switchable	R8	–	DV_{DD}	–
CVDD	SPI supply – Switchable	M8	–	CV_{DD}	–
EVDD	eSDHC supply – Switchable	L8	–	EV_{DD}	–
L1VDD1	Ethernet controller 1 and GPIO supply- Always ON	T8	–	$L1V_{DD}$	–
L1VDD2	Ethernet controller 1 and GPIO supply- Always ON	U8	–	$L1V_{DD}$	–
LVDD1	Ethernet controller 2, 1588 and GPIO supply – Switchable	V8	–	LV_{DD}	–
LVDD2	Ethernet controller 2, 1588 and GPIO supply – Switchable	W8	–	LV_{DD}	–
S1VDD1	SerDes 1 core logic supply – Switchable	W15	–	$S1V_{DD}$	–
S1VDD2	SerDes 1 core logic supply – Switchable	W16	–	$S1V_{DD}$	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S1VDD3	SerDes 1 core logic supply – Switchable	W17	–	$S1V_{DD}$	–
S1VDD4	SerDes 1 core logic supply – Switchable	W18	–	$S1V_{DD}$	–
S1VDD5	SerDes 1 core logic supply – Switchable	W19	–	$S1V_{DD}$	–
S1VDD6	SerDes 1 core logic supply – Switchable	W20	–	$S1V_{DD}$	–
S1VDD7	SerDes 1 core logic supply – Switchable	Y13	–	$S1V_{DD}$	–
X1VDD1	SerDes 1 transceiver supply – Switchable	AC9	–	$X1V_{DD}$	–
X1VDD2	SerDes 1 transceiver supply – Switchable	AC12	–	$X1V_{DD}$	–
X1VDD3	SerDes 1 transceiver supply – Switchable	AC15	–	$X1V_{DD}$	–
X1VDD4	SerDes 1 transceiver supply – Switchable	AC18	–	$X1V_{DD}$	–
X1VDD5	SerDes 1 transceiver supply – Switchable	AC21	–	$X1V_{DD}$	–
PROG_SFP	SFP Fuse Programming supply	F12	–	PROG_SFP	–
TH_VDD	Thermal Monitor Unit supply – Switchable	G9	–	TH_V_{DD}	–
VDD01	Supply for cores and platform – Switchable	K15	–	V_{DD}	–
VDD02	Supply for cores and platform – Switchable	K17	–	V_{DD}	–
VDD03	Supply for cores and platform – Switchable	K19	–	V_{DD}	–
VDD04	Supply for cores and platform – Switchable	L12	–	V_{DD}	–
VDD05	Supply for cores and platform – Switchable	L14	–	V_{DD}	–
VDD06	Supply for cores and platform – Switchable	L16	–	V_{DD}	–
VDD07	Supply for cores and platform – Switchable	L18	–	V_{DD}	–
VDD08	Supply for cores and platform – Switchable	L20	–	V_{DD}	–
VDD09	Supply for cores and platform – Switchable	M13	–	V_{DD}	–
VDD10	Supply for cores and platform – Switchable	M15	–	V_{DD}	–
VDD11	Supply for cores and platform – Switchable	M17	–	V_{DD}	–
VDD12	Supply for cores and platform – Switchable	M19	–	V_{DD}	–
VDD13	Supply for cores and platform – Switchable	N12	–	V_{DD}	–
VDD14	Supply for cores and platform – Switchable	N14	–	V_{DD}	–
VDD15	Supply for cores and platform – Switchable	N16	–	V_{DD}	–
VDD16	Supply for cores and platform – Switchable	N18	–	V_{DD}	–
VDD17	Supply for cores and platform – Switchable	N20	–	V_{DD}	–
VDD18	Supply for cores and platform – Switchable	P11	–	V_{DD}	–
VDD19	Supply for cores and platform – Switchable	P13	–	V_{DD}	–
VDD20	Supply for cores and platform – Switchable	P15	–	V_{DD}	–
VDD21	Supply for cores and platform – Switchable	P17	–	V_{DD}	–
VDD22	Supply for cores and platform – Switchable	P19	–	V_{DD}	–
VDD23	Supply for cores and platform – Switchable	R12	–	V_{DD}	–
VDD24	Supply for cores and platform – Switchable	R14	–	V_{DD}	–
VDD25	Supply for cores and platform – Switchable	R16	–	V_{DD}	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD26	Supply for cores and platform – Switchable	R18	–	VDD	–
VDD27	Supply for cores and platform – Switchable	R20	–	VDD	–
VDD28	Supply for cores and platform – Switchable	T13	–	VDD	–
VDD29	Supply for cores and platform – Switchable	T15	–	VDD	–
VDD30	Supply for cores and platform – Switchable	T17	–	VDD	–
VDD31	Supply for cores and platform – Switchable	T19	–	VDD	–
VDD32	Supply for cores and platform – Switchable	U14	–	VDD	–
VDD33	Supply for cores and platform – Switchable	U16	–	VDD	–
VDD34	Supply for cores and platform – Switchable	U18	–	VDD	–
VDD35	Supply for cores and platform – Switchable	U20	–	VDD	–
VDD36	Supply for cores and platform – Switchable	V13	–	VDD	–
VDD37	Supply for cores and platform – Switchable	V15	–	VDD	–
VDD38	Supply for cores and platform – Switchable	V17	–	VDD	–
VDD39	Supply for cores and platform – Switchable	V19	–	VDD	–
VDD40	Supply for cores and platform – Switchable	W14	–	VDD	–
VDDC01	Always ON supply	K11	–	VDDC	–
VDDC02	Always ON supply	K13	–	VDDC	–
VDDC03	Always ON supply	L10	–	VDDC	–
VDDC04	Always ON supply	M11	–	VDDC	–
VDDC05	Always ON supply	N10	–	VDDC	–
VDDC06	Always ON supply	R10	–	VDDC	–
VDDC07	Always ON supply	T11	–	VDDC	–
VDDC08	Always ON supply	U10	–	VDDC	–
VDDC09	Always ON supply	U12	–	VDDC	–
VDDC10	Always ON supply	V11	–	VDDC	–
VDDC11	Always ON supply	W10	–	VDDC	–
VDDC12	Always ON supply	W12	–	VDDC	–
AVDD_CGA1	e5500 Cluster Group A PLL1 supply (SDHC/Cores fed through this) – Switchable	G11	–	AVDD_CGA1	–
AVDD_CGA2	e5500 Cluster Group A PLL2 supply (Cores are fed through this) – Switchable	G12	–	AVDD_CGA2	–
AVDD_PLAT	Platform PLL supply – Always ON	G10	–	AVDD_PLAT	–
AVDD_D1	DDR1 PLL supply – Switchable	E20	–	AVDD_D1	–
AVDD_SD1_PLL1	SerDes1 PLL 1 supply – Switchable	AB16	–	AVDD_SD1_PLL1	–
AVDD_SD1_PLL2	SerDes1 PLL 2 supply – Switchable	AB20	–	AVDD_SD1_PLL2	–
SENSEVDD	Vdd Sense pin – Switchable	G19	–	SENSEVDD	–

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SENSEVDDC	Vddc Sense pin – Always ON	AB9	–	SENSEVDDC	–
USB_HVDD1	USB PHY Transceiver 3.3V Supply – "Optionally Switchable or Always ON"	J8	–	USB_HV_{DD}	–
USB_HVDD2	USB PHY Transceiver 3.3V Supply – "Optionally Switchable or Always ON"	K8	–	USB_HV_{DD}	–
USB_OVDD1	USB PHY Transceiver 1.8V Supply – "Optionally Switchable or Always ON"	J9	–	USB_OV_{DD}	–
USB_OVDD2	USB PHY Transceiver 1.8V Supply – "Optionally Switchable or Always ON"	J10	–	USB_OV_{DD}	–
USB_SVDD1	USB PHY Analog 1.0V Supply – "Optionally Switchable or Always ON"	K9	–	USB_SV_{DD}	–
USB_SVDD2	USB PHY Analog 1.0V Supply – "Optionally Switchable or Always ON"	K10	–	USB_SV_{DD}	–
G1VDD	DDR supply for port 1 – Switchable	B23			
G1VDD	DDR supply for port 1 – Switchable	B25			
G1VDD	DDR supply for port 1 – Switchable	C22			
G1VDD	DDR supply for port 1 – Switchable	C26			
G1VDD	DDR supply for port 1 – Switchable	E22			
G1VDD	DDR supply for port 1 – Switchable	E26			
G1VDD	DDR supply for port 1 – Switchable	G22			
G1VDD	DDR supply for port 1 – Switchable	G26			
G1VDD	DDR supply for port 1 – Switchable	J22			
G1VDD	DDR supply for port 1 – Switchable	J26			
G1VDD	DDR supply for port 1 – Switchable	L22			
G1VDD	DDR supply for port 1 – Switchable	L26			
G1VDD	DDR supply for port 1 – Switchable	N22			
G1VDD	DDR supply for port 1 – Switchable	N26			
G1VDD	DDR supply for port 1 – Switchable	R22			
G1VDD	DDR supply for port 1 – Switchable	R26			
G1VDD	DDR supply for port 1 – Switchable	U24			
G1VDD	DDR supply for port 1 – Switchable	W24			
G1VDD	DDR supply for port 1 – Switchable	AA24			
G1VDD	DDR supply for port 1 – Switchable	AC24			
G1VDD	DDR supply for port 1 – Switchable	AC26			
G1VDD	DDR supply for port 1 – Switchable	AE24			
G1VDD	DDR supply for port 1 – Switchable	AE26			
G1VDD	DDR supply for port 1 – Switchable	AG22			
G1VDD	DDR supply for port 1 – Switchable	AG26			
G1VDD	DDR supply for port 1 – Switchable	AG28			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD	DDR supply for port 1 – Switchable	AH27			
G1VDD	DDR supply for port 1 – Switchable	A22			
G1VDD	DDR supply for port 1 – Switchable	A24			
G1VDD	DDR supply for port 1 – Switchable	A26			
G1VDD	DDR supply for port 1 – Switchable	A28			
G1VDD	DDR supply for port 1 – Switchable	A30			
G1VDD	DDR supply for port 1 – Switchable	A32			
G1VDD	DDR supply for port 1 – Switchable	A34			
G1VDD	DDR supply for port 1 – Switchable	A36			
G1VDD	DDR supply for port 1 – Switchable	A38			
G1VDD	DDR supply for port 1 – Switchable	A40			
G1VDD	DDR supply for port 1 – Switchable	A42			
G1VDD	DDR supply for port 1 – Switchable	A44			
G1VDD	DDR supply for port 1 – Switchable	B21			
G1VDD	DDR supply for port 1 – Switchable	B27			
G1VDD	DDR supply for port 1 – Switchable	B29			
G1VDD	DDR supply for port 1 – Switchable	B31			
G1VDD	DDR supply for port 1 – Switchable	B33			
G1VDD	DDR supply for port 1 – Switchable	B35			
G1VDD	DDR supply for port 1 – Switchable	B37			
G1VDD	DDR supply for port 1 – Switchable	B39			
G1VDD	DDR supply for port 1 – Switchable	B41			
G1VDD	DDR supply for port 1 – Switchable	B43			
G1VDD	DDR supply for port 1 – Switchable	C24			
G1VDD	DDR supply for port 1 – Switchable	C28			
G1VDD	DDR supply for port 1 – Switchable	C30			
G1VDD	DDR supply for port 1 – Switchable	C32			
G1VDD	DDR supply for port 1 – Switchable	C34			
G1VDD	DDR supply for port 1 – Switchable	C36			
G1VDD	DDR supply for port 1 – Switchable	C38			
G1VDD	DDR supply for port 1 – Switchable	C40			
G1VDD	DDR supply for port 1 – Switchable	C42			
G1VDD	DDR supply for port 1 – Switchable	C44			
G1VDD	DDR supply for port 1 – Switchable	D23			
G1VDD	DDR supply for port 1 – Switchable	D25			
G1VDD	DDR supply for port 1 – Switchable	D27			
G1VDD	DDR supply for port 1 – Switchable	E24			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD	DDR supply for port 1 – Switchable	E28			
G1VDD	DDR supply for port 1 – Switchable	F21			
G1VDD	DDR supply for port 1 – Switchable	F23			
G1VDD	DDR supply for port 1 – Switchable	F25			
G1VDD	DDR supply for port 1 – Switchable	F27			
G1VDD	DDR supply for port 1 – Switchable	F28			
G1VDD	DDR supply for port 1 – Switchable	G24			
G1VDD	DDR supply for port 1 – Switchable	G28			
G1VDD	DDR supply for port 1 – Switchable	H21			
G1VDD	DDR supply for port 1 – Switchable	H23			
G1VDD	DDR supply for port 1 – Switchable	H25			
G1VDD	DDR supply for port 1 – Switchable	H27			
G1VDD	DDR supply for port 1 – Switchable	J24			
G1VDD	DDR supply for port 1 – Switchable	J28			
G1VDD	DDR supply for port 1 – Switchable	K21			
G1VDD	DDR supply for port 1 – Switchable	K23			
G1VDD	DDR supply for port 1 – Switchable	K25			
G1VDD	DDR supply for port 1 – Switchable	K27			
G1VDD	DDR supply for port 1 – Switchable	L21			
G1VDD	DDR supply for port 1 – Switchable	L24			
G1VDD	DDR supply for port 1 – Switchable	M21			
G1VDD	DDR supply for port 1 – Switchable	M23			
G1VDD	DDR supply for port 1 – Switchable	M25			
G1VDD	DDR supply for port 1 – Switchable	M27			
G1VDD	DDR supply for port 1 – Switchable	N21			
G1VDD	DDR supply for port 1 – Switchable	N24			
G1VDD	DDR supply for port 1 – Switchable	N28			
G1VDD	DDR supply for port 1 – Switchable	P21			
G1VDD	DDR supply for port 1 – Switchable	P23			
G1VDD	DDR supply for port 1 – Switchable	P25			
G1VDD	DDR supply for port 1 – Switchable	P27			
G1VDD	DDR supply for port 1 – Switchable	R21			
G1VDD	DDR supply for port 1 – Switchable	R24			
G1VDD	DDR supply for port 1 – Switchable	R28			
G1VDD	DDR supply for port 1 – Switchable	T21			
G1VDD	DDR supply for port 1 – Switchable	T23			
G1VDD	DDR supply for port 1 – Switchable	T25			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD	DDR supply for port 1 – Switchable	T27			
G1VDD	DDR supply for port 1 – Switchable	U21			
G1VDD	DDR supply for port 1 – Switchable	U22			
G1VDD	DDR supply for port 1 – Switchable	U26			
G1VDD	DDR supply for port 1 – Switchable	V21			
G1VDD	DDR supply for port 1 – Switchable	V23			
G1VDD	DDR supply for port 1 – Switchable	V25			
G1VDD	DDR supply for port 1 – Switchable	W21			
G1VDD	DDR supply for port 1 – Switchable	W22			
G1VDD	DDR supply for port 1 – Switchable	W26			
G1VDD	DDR supply for port 1 – Switchable	W27			
G1VDD	DDR supply for port 1 – Switchable	W28			
G1VDD	DDR supply for port 1 – Switchable	Y21			
G1VDD	DDR supply for port 1 – Switchable	Y23			
G1VDD	DDR supply for port 1 – Switchable	Y25			
G1VDD	DDR supply for port 1 – Switchable	Y27			
G1VDD	DDR supply for port 1 – Switchable	Y28			
G1VDD	DDR supply for port 1 – Switchable	AA22			
G1VDD	DDR supply for port 1 – Switchable	AA26			
G1VDD	DDR supply for port 1 – Switchable	AA27			
G1VDD	DDR supply for port 1 – Switchable	AA28			
G1VDD	DDR supply for port 1 – Switchable	AB23			
G1VDD	DDR supply for port 1 – Switchable	AB25			
G1VDD	DDR supply for port 1 – Switchable	AB27			
G1VDD	DDR supply for port 1 – Switchable	AC22			
G1VDD	DDR supply for port 1 – Switchable	AC28			
G1VDD	DDR supply for port 1 – Switchable	AD23			
G1VDD	DDR supply for port 1 – Switchable	AD25			
G1VDD	DDR supply for port 1 – Switchable	AD27			
G1VDD	DDR supply for port 1 – Switchable	AE22			
G1VDD	DDR supply for port 1 – Switchable	AE28			
G1VDD	DDR supply for port 1 – Switchable	AF23			
G1VDD	DDR supply for port 1 – Switchable	AF25			
G1VDD	DDR supply for port 1 – Switchable	AF27			
G1VDD	DDR supply for port 1 – Switchable	AF29			
G1VDD	DDR supply for port 1 – Switchable	AF31			
G1VDD	DDR supply for port 1 – Switchable	AF33			

Table 2-1. Pinout List (Continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD	DDR supply for port 1 – Switchable	AF35			
G1VDD	DDR supply for port 1 – Switchable	AF37			
G1VDD	DDR supply for port 1 – Switchable	AF39			
G1VDD	DDR supply for port 1 – Switchable	AF41			
G1VDD	DDR supply for port 1 – Switchable	AF43			
G1VDD	DDR supply for port 1 – Switchable	AG24			
G1VDD	DDR supply for port 1 – Switchable	AG30			
G1VDD	DDR supply for port 1 – Switchable	AG32			
G1VDD	DDR supply for port 1 – Switchable	AG34			
G1VDD	DDR supply for port 1 – Switchable	AG36			
G1VDD	DDR supply for port 1 – Switchable	AG38			
G1VDD	DDR supply for port 1 – Switchable	AG40			
G1VDD	DDR supply for port 1 – Switchable	AG42			
G1VDD	DDR supply for port 1 – Switchable	AG44			
G1VDD	DDR supply for port 1 – Switchable	AH23			
G1VDD	DDR supply for port 1 – Switchable	AH25			
G1VDD	DDR supply for port 1 – Switchable	AH29			
G1VDD	DDR supply for port 1 – Switchable	AH31			
G1VDD	DDR supply for port 1 – Switchable	AH33			
G1VDD	DDR supply for port 1 – Switchable	AH35			
G1VDD	DDR supply for port 1 – Switchable	AH37			
G1VDD	DDR supply for port 1 – Switchable	AH39			
G1VDD	DDR supply for port 1 – Switchable	AH41			
G1VDD	DDR supply for port 1 – Switchable	AH43			
DDR_VTT	DDR VTT	U27	–		–
DDR_VTT	DDR VTT	U28			
DDR_VTT	DDR VTT	V27			
DDR_VTT	DDR VTT	V28			
No Connection Pins					
NC01	No Connection	L6	–	–	–
NC02	No Connection	M6	–	–	–
NC03	No Connection	P6	–	–	–
NC04	No Connection	R6	–	–	–

Notes: 1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin is therefore be described as an I/O for boundary scan.

2. During reset this output signal is actively driven rather than being tri-stated.

3. MDIC[0] is grounded through a 162Ω precision 1% resistor and MDIC[1] is connected to GV1DD through a 162Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162Ω. Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3L IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors.
4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.
5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.
7. This pin is an open-drain signal.
8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.
9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.
10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.
11. This pin requires a 200Ω pull-up to respective power-supply.
12. Do not connect. These pins should be left floating.
13.
14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
15. These pins must be pulled to ground (GND).
16. This pin requires a 698Ω pull-up to respective power-supply.
17. This pin should be connected to ground through 2-10kΩ resistor when not used.
18. This pin should be connected to ground through 2-10kΩ resistor when SYSCLK input is used as system clock.
19. This pin should be tied to ground if the diode is not utilized for temperature monitoring.
20. This pin should be connected to GND through a 10kΩ ± 1% resistor with a low temperature coefficient of ≤ 25ppm/×C for bias generation
21. This pin has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pin should have an optional pull down resistor on board. This is required to support DIFF_SYSCLK/DIFF_SYSCLK_B
22. This pin should not be sampled until PORESET_B gets deasserted.
23. This pin must be pulled to O1VDD through a 100-ohm to 1k-ohm resistor for a 4 core QT1040 and tied to ground for a 2 core QT1020 device.
24. External “CLK12” pin is connected internally to both CLK12 and CLK8 pins of QE.
25. PORESET_B should be asserted zero during the JTAG Boundary scan operation, and is required to be controllable on board.
26. This pin requires a pull-up to the respective power supply so as to meet the timing requirements in Table 3-20.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3. ELECTRICAL CHARACTERISTICS

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 3-1. Absolute maximum ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	–0.3 to 1.1	V	[9]
Always ON supply voltage	V_{DDC}	–0.3 to 1.1	V	–
PLL supply voltage (core PLL/eSDHC, platform, DDR)	AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_PLAT AV_{DD}_D1	–0.3 to 1.98	V	[10]
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)	AVDD_SD1_PLL1 AVDD_SD1_PLL2	–0.3 to 1.48	V	–
SFP fuse programming	PROG_SFP	–0.3 to 1.98	V	–
Thermal monitor unit supply	TH_V_{DD}	–0.3 to 1.98	V	–
MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	OV_{DD} $O1V_{DD}$	–0.3 to 1.98	V	–
DUART, I^2C, DMA, TDM, QE, MPIC, DIU	DV_{DD}	–0.3 to 2.75 –0.3 to 1.98 –0.3 to 3.63	V	–
eSPI, SDHC_WP, SDHC_CD, SDHC_DAT[4:7]	CV_{DD}	–0.3 to 1.98 –0.3 to 3.63	V	–
eSDHC	EV_{DD}	–0.3 to 1.98 –0.3 to 3.63	V	–
DDR3L DRAM I/O voltage (DDR3L)	$G1V_{DD}$	–0.3 to 1.48		
DDR3L Termination	V_{TT}	–0.2 to 0.74	V	–
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	$S1V_{DD}$	–0.3 to 1.1	V	–
Pad power supply for SerDes transmitter	$X1V_{DD}$	–0.3 to 1.48	V	–
Ethernet interface 2, 1588, GPIO	LV_{DD}	–0.3 to 1.98 –0.3 to 2.75 –0.3 to 3.63	V	–
Ethernet interface 1, Ethernet management interface 1 (EMI1), GPIO	$L1V_{DD}$	–0.3 to 1.98 –0.3 to 2.75 –0.3 to 3.63	V	–
USB PHY Transceiver supply voltage	USB_HV_{DD}	–0.3 to 3.63	V	–
	USB_OV_{DD}	–0.3 to 1.98	V	–

Table 3-1. Absolute maximum ratings[(1)] (Continued)

Characteristic		Symbol	Max Value	Unit	Notes
USB PHY Analog supply voltage		USB_SV_{DD}	–0.3 to 1.1	V	–
Input voltage	DDR3L DRAM signals	MV_{IN}	–0.3 to ($G1V_{DD}$ + 0.3)	V	(2)
	DDR3L DRAM reference	$D1\_MV_{REF}$	–0.3 to ($G1V_{DD}$/2 + 0.3)	V	(5)
	Ethernet signals	LV_{IN} $LV1_{IN}$	–0.3 to (LnV_{DD} + 0.3)	V	(4)(5)
	MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	OV_{IN} $O1V_{IN}$	–0.3 to (OnV_{DD} + 0.3)	V	(3)(5)
	eSDHC signals	EV_{IN}	–0.3 to (EV_{DD} + 0.3)	V	(7)(5)
	eSPI signals	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	(8)(5)
	DUART, I²C, DMA, TDM, QE, MPIC, DIU	DV_{IN}	–0.3 to (DV_{DD} + 0.3)	V	(5)(6)
	SerDes signals	$S1V_{IN}$	–0.4 to ($S1V_{DD}$ + 0.3)	V	(5)
	USB PHY Transceiver signals	USB_HV_{IN}	–0.3 to (USB_HV_{DD} + 0.3)	V	(5)
		USB_OV_{IN}	–0.3 to (USB_OV_{DD} + 0.3)	V	(5)
Storage temperature range		T_{STG}	–55 to 150	°C	–

Notes:
1. Functional operating conditions are given in Table 3-2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed $G1V_{DD}$ by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (S,G,L,O,D,E,C)V_{IN}, USBn_V_{IN}_3P3, USBn_V_{IN}_1P8 and Dn_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3-1.
6. **Caution:** DV_{IN} must not exceed DV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. **Caution:** EV_{IN} must not exceed EV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
10. AVDD_PLAT, AVDD_CGA1, AVDD_CGA2 and AVDD_D1 are measured at the input to the filter (as shown in AN4825) and not at the pin of the device.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE
The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3-2. Recommended operating conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage	V_{DD}	1.0 ± 30 mV	V	(3)(4)(5)
Always ON Core and Platform supply	V_{DDC}	1.0 ± 30 mV	V	(3)(4)(5)
PLL supply voltage (core PLL/eSDHC, platform, DDR)	AV_{DD}_CGA1	1.8V ± 90 mV	V	–
	AV_{DD}_CGA2			
	AV_{DD}_PLAT			
	AV_{DD}_D1			
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)	AV_{DD}_SD1_PLL1 AV_{DD}_SD1_PLL2	1.35V ± 67 mV	V	–
SFP fuse programming	PROG_SFP	1.8V ± 90 mV	V	(2)
Thermal monitor unit supply	TH_V_{DD}	1.8V ± 90 mV	V	–
IFC, GPIO, Trust, DDRCLK supply, RTC and JTAG I/O voltage	OV_{DD}	1.8V ± 90 mV	V	–
MPIC, GPIO, system control, debug and SYSCLK supply	$O1V_{DD}$	1.8V ± 90 mV	V	–
DUART, I^2C, DMA, MPIC, QE, TDM, DIU	DV_{DD}	2.5V ± 125 mV 1.8V ± 90 mV 3.3V ± 165 mV	V	–
eSPI, SDHC_WP, SDHC_CD, SDHC_DAT[4:7]	CV_{DD}	3.3V ± 165mV 1.8V ± 90mV	V	–
eSDHC	EV_{DD}	3.3V ±165 mV 1.8V ± 90 mV	V	–
DDR DRAM I/O voltage — DDR3L	$G1V_{DD}$	1.35V ± 67 mV		
DDR3L Termination	V_{TT}	$G1V_{DD}/2$ ± 1%	V	(6)
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	$S1V_{DD}$	1.0V + 50 mV 1.0V – 30 mV	V	–
Pad power supply for SerDes transmitters	$X1V_{DD}$	1.35V ± 67 mV	V	–
Ethernet interface 2, 1588, GPIO	LV_{DD}	1.8V ± 90 mV 2.5V ± 125 mV 3.3V ± 165 mV	V	(1)
Ethernet interface 1, Ethernet management interface 1 (EMI1), GPIO	$L1V_{DD}$	1.8V ± 90 mV 2.5V ± 125 mV 3.3V ± 165 mV	V	(1)
USB PHY Transceiver supply voltage	USB_HV_{DD}	3.3V ± 165 mV	V	–
	USB_OV_{DD}	1.8V ± 90 mV	V	–
USB PHY Analog supply voltage	USB_SV_{DD}	1.0 ± 50mV	V	(3)

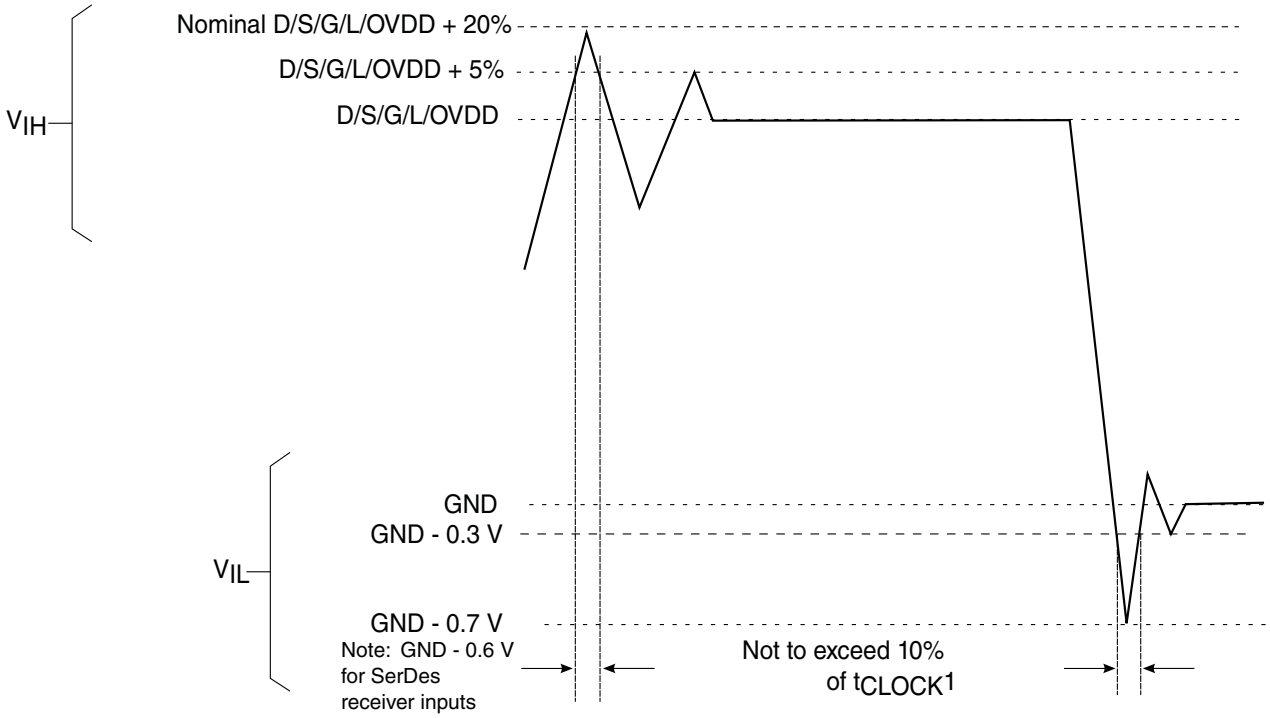
Table 3-2. Recommended operating conditions (Continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Input voltage	DDR3L DRAM signals	MV_{IN}	GND to $G1V_{DD}$	V	–
	DDR3L DRAM reference	$D1\_MV_{REF}$	$G1V_{DD}/2 \pm 1\%$	V	–
	Ethernet interface, EMI1, 1588, GPIO	LV_{IN} L1V	GND to LV_{DD} GND to L1V	V	–
	MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	OV_{IN} $O1V_{IN}$	GND to OnV_{DD}	V	–
	DUART, I^2C, DMA, TDM, QE, MPIC, DIU	DV_{IN}	GND to DV_{DD}	V	–
	eSDHC, eSPI	CV_{IN}, EV_{IN}	GND to CV_{DD}/EV_{DD}	V	–
	SerDes signals	SV_{IN}	GND to $S1V_{DD}$	V	–
	USB PHY Transceiver signals	USB_HV_{IN}	GND to USB_HV_{DD}	V	–
		USB_OV_{IN}	GND to USB_OV_{DD}	V	–
Operating temperature range	Industrial	T_C, T_J	T_C = –40 (min) to T_J = 110 (max)	°C	–
	Military	T_C, T_J	T_C = –55 (min) to T_J = 125(max)	°C	–
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	(2)

Notes:
1. Selecting RGMII limits L1VDD and LVDD = 1.8V or 2.5V. L1VDD and LVDD should be configured at same voltage.
2. PROG_SFP must be supplied 1.8V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.
3. Refer to Core and platform supply voltage filtering for additional information.
4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
5. Operation at 1.1V is allowable for up to 25ms at initial power on.
6. This power supply needs a sink and source regulator

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

Figure 3-1. Overshoot/Undershoot voltage for $G1V_{DD}/L1V_{DD}/OV_{DD}/SV_{DD}/DV_{DD}/CV_{DD}/LV_{DD}/EV_{DD}$



Notes:

t_{CLOCK} refers to the clock period associated with the respective interface:

For I^2C OV_{DD}, t_{CLOCK} references SYSCLK.

For DDR GV_{DD}, t_{CLOCK} references Dn_MCLK.

For eSPI OV_{DD}, t_{CLOCK} references SPI_CLK.

For JTAG OV_{DD}, t_{CLOCK} references TCK.

For SerDes SVDD, t_{CLOCK} references SD_REF_CLK.

For Ethernet LV_{DD}, t_{CLOCK} references ECn_GTX_CLK125.

See Table 3-2 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3-2. The input voltage threshold scales with respect to the associated I/O supply voltage. DV_{DD}, OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MV_{REF} signal (nominally set to $G1V_{DD}/2$) as is appropriate for the SSTL_1.35/SSTL_1.2 electrical signaling standard. The DDR MDQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE
These values are preliminary estimates.

Table 3-3. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR3L signal	–	18(full-strength mode) 27(half-strength mode)	–	$G1V_{DD}$ = 1.35V	[1]
Ethernet signals	45	–	90	$L1V_{DD}$/ LV_{DD} = 3.3V	–
	40	–	90	$L1V_{DD}$/ LV_{DD} = 2.5V	
	40	–	75	$L1V_{DD}$/ LV_{DD} = 1.8V	
MPIC, GPIO, system control and power management, clocking, debug, IFC,DDRCLK supply, and JTAG I/O voltage	23	–	51	OV_{DD}, $O1V_{DD}$ = 1.8V	–
DUART, DMA, MPIC, QE, TDM, I^2C, DIU	45	–	90	DV_{DD} = 3.3V	–
	40	–	90	DV_{DD} = 2.5V	
	40	–	75	DV_{DD} = 1.8V	
eSPI, SDHC_WP, SDHC_CD	45	–	90	CV_{DD} = 3.3V	–
	40	–	75	CV_{DD} = 1.8V	
eSDHC	45	–	90	EV_{DD} = 3.3V	–
	40	–	75	EV_{DD} = 1.8V	

Notes:
1. The drive strength of the DDR3L interface in half-strength mode is at T_j = 105 °C and at $G1V_{DD}$ (min).
2. Estimated number based on best case processed device.
3. Estimated number based on worst case processed device.

3.1.4 General AC timing specifications

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 3-4. AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	–	5	ns	[1]

Note:
1. Rise time refers to signal transitions from 10% to 90% of Supply; fall time refers to transitions from 90% to 10% of supply

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation.

Power up sequence when DDR3L is used

1. $O1V_{DD}$, OV_{DD}, DV_{DD}, CV_{DD}, EV_{DD}, $L1V_{DD}$, LV_{DD}, TH_V_{DD}, USB_HV_{DD}, USB_OV_{DD}, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1. Drive PROG_SFP = GND
   a. PORESET_B should be driven asserted and held during this step.
2. V_{DDC}, V_{DD}, USB_SV_{DD}, $S1V_{DD}$
   a. When Deep Sleep is not used, it is recommended to source V_{DD} and V_{DDC} from same power supply.
3. $G1V_{DD}$, $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2
   a. All supplies in Step 3 may be sourced from same supply

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

All supplies must be at their stable values within 75 ms.

Negate PORESET_B input when the required assertion/hold time has been met per Table 3-20.

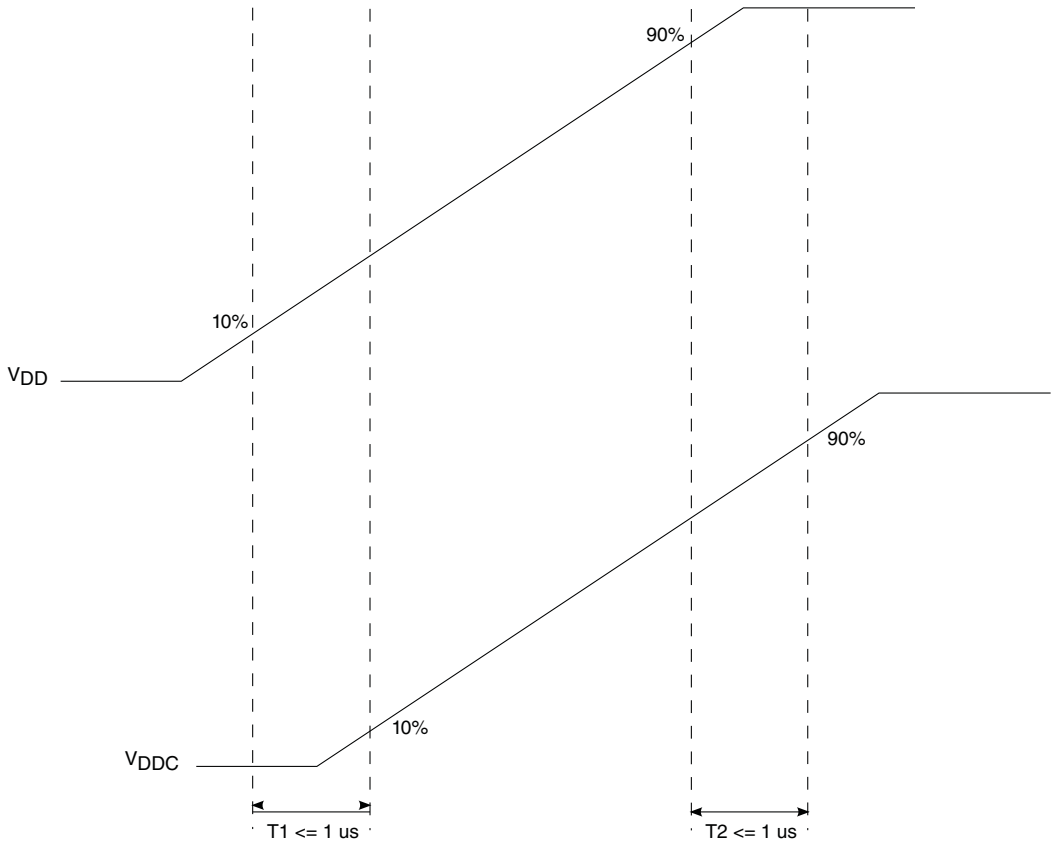
NOTE

- EVT2_B may be unstable when PORESET_B is asserted. The signal should not be used to enable switchable power supplies during this period.
- Ramp rate requirements should be met per Table 3-6

  Warning
  Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.
- Due to the internal design of the QT1040, the deep sleep mode is not available.

This figure provides the V_{DDC} and V_{DD} ramp up diagram.

Figure 3-2. V_{DDC} and V_{DD} ramp up diagram



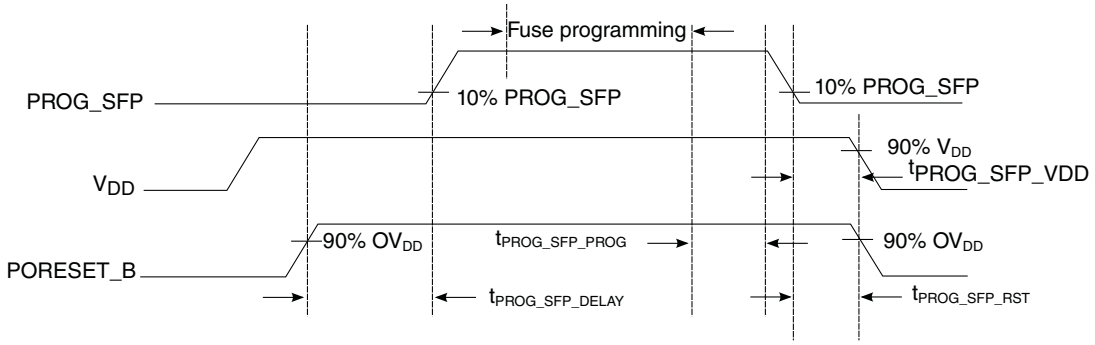
For secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive PROG_SFP = 1.8V after a required minimum delay per Table 3-5.
2. After fuse programming is completed, it is required to return PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 3-5. See Security fuse processor, for additional details.

Warning
No activity other than that required for secure boot fuse programming is permitted while PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND.

This figure provides the PROG_SFP timing diagram.

Figure 3-3. PROG_SFP timing diagram



Note: PROG_SFP must be stable at 1.8V prior to initiating fuse programming.

This table provides information on the power-down and power-up sequence parameters for PROG_SFP.

Table 3-5. PROG_SFP timing[5]

Driver type	Min	Max	Unit	Notes
$t_{PROG\_SFP\_DELAY}$	100	–	SYSCLKs	(1)
$t_{PROG\_SFP\_PROG}$	0	–	µs	(2)
$t_{PROG\_SFP\_VDD}$	0	–	µs	(3)
$t_{PROG\_SFP\_RST}$	0	–	µs	(4)

Notes:
1. Delay required from the deassertion of PORESET_B to driving PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% PROG_SFP ramp up.
2. Delay required from fuse programming finished to PROG_SFP ramp down start. Fuse programming must complete while PROG_SFP is stable at 1.8V. No activity other than that required for secure boot fuse programming is permitted while PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND. After fuse programming is completed, it is required to return PROG_SFP = GND.
3. Delay required from PROG_SFP ramp down complete to V_{DD} ramp down start. PROG_SFP must be grounded to minimum 10% PROG_SFP before V_{DD} is at 90% V_{DD}.
4. Delay required from PROG_SFP ramp down complete to PORESET_B assertion. PROG_SFP must be grounded to minimum 10% PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 3-5.

3.4 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.
This table provides the power supply ramp rate specifications.

Table 3-6. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/$O1V_{DD}$/DV_{DD}/ $G1V_{DD}$/$S1V_{DD}$/$X1V_{DD}$/LV_{DD}/$L1V_{DD}$/EV_{DD}/CV_{DD} all core and platform V_{DD} supplies, D1_MV_{REF} and all AV_{DD} supplies.)	–	25	V/ms	(1)(2)
Required ramp rate for PROG_SFP	–	25	V/ms	(1)(2)
Required ramp rate for USB_HV_{DD}	–	26.7	V/ms	(1)(2)

Notes: 1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3-2).

3.5 Power characteristics

This table shows the power dissipations of the V_{DD} and V_{DDC} supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 3-7. QT1040 core power dissipation

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD}, V_{DDC} (V)	$S1V_{DD}$ (V)	Junction temp. (ºC)	Power mode	Power (W)			Total Core and platform power (W)(1)	Notes
							V_{DD}	V_{DDC}	$S1V_{DD}$		
1500	600	1600	1.0	1.0	65	Typical	5.44	0.63	0.41	6.48	(2)(3)
					105	Thermal	7.51	0.91	0.47	8.89	(5)(7)
						Maximum	8.26	0.91	0.47	9.64	(4)(6)(7)
					125	Thermal	9.29	1.09	0.49	10.87	(5)(7)
						Maximum	10.05	1.09	0.49	11.63	(4)(6)(7)
1400	600	1600	1.0	1.0	65	Typical	5.62	0.63	0.41	6.66	(2)(3)
					105	Thermal	6.24	0.69	0.41	7.34	(5)(7)
						Maximum	6.97	0.69	0.41	8.07	(4)(6)(7)
					125	Thermal	7.61	0.87	0.43	8.91	(5)(7)
						Maximum	8.34	0.87	0.43	9.64	(4)(6)(7)
1200	500	1600	1.0	1.0	65	Typical	4.86	0.57	0.41	5.84	(2)(3)
					105	Thermal	5.52	0.63	0.41	6.56	(5)(7)
						Maximum	6.12	0.63	0.41	7.16	(4)(6)(7)
					125	Thermal	6.89	0.81	0.43	8.13	(5)(7)
						Maximum	7.49	0.81	0.43	8.73	(4)(6)(7)

Notes: 1. Combined power of VDDC, VDD and S1VDD with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and is executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.

4. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

Table 3-8. QT1020 core power dissipation

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD}, V_{DDC} (V)	$S1V_{DD}$ (V)	Junction temp. (ºC)	Power mode	Power (W)			Total Core and platform power (W)(1)	Notes
							V_{DD}	V_{DDC}	$S1V_{DD}$		
1500	600	1600	1.0	1.0	65	Typical	4.58	0.63	0.41	5.62	(2)(3)
					105	Thermal	6.41	0.91	0.47	7.79	(5)(7)
						Maximum	6.99	0.91	0.47	8.37	(4)(6)(7)
					125	Thermal	7.78	1.09	0.49	9.36	(5)(7)
						Maximum	8.36	1.09	0.49	9.94	(4)(6)(7)
1400	600	1600	1.0	1.0	65	Typical	4.52	0.63	0.41	5.56	(2)(3)
					105	Thermal	5.05	0.69	0.41	6.15	(5)(7)
						Maximum	5.61	0.69	0.41	6.71	(4)(6)(7)
					125	Thermal	6.42	0.87	0.43	7.72	(5)(7)
						Maximum	6.98	0.87	0.43	8.28	(4)(6)(7)
1200	500	1600	1.0	1.0	65	Typical	3.90	0.57	0.41	4.88	(2)(3)
					105	Thermal	4.42	0.63	0.41	5.46	(5)(7)
						Maximum	4.89	0.63	0.41	5.93	(4)(6)(7)
					125	Thermal	5.79	0.81	0.43	7.03	(5)(7)
						Maximum	6.26	0.81	0.43	7.50	(4)(6)(7)

Notes:
1. Combined power of VDDC, VDD and S1VDD with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and is executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table provides low power mode saving estimation.

Table 3-9. Single core, Single cluster low power mode power savings, 1.0V 65°C[1][2][3]

Mode	Core Frequency = 1.0 GHz	Core Frequency = 1.2 GHz	Core Frequency = 1.4 GHz	Units	Comment	Notes
PH10	0.19	0.23	0.27	Watts	Saving realized moving from PH00 to PH10 state, single core.	(4)
PH15	0.19	0.23	0.27	Watts	Saving realized moving from PH10 state to PH15 state, single core.	(4)
LPM20	0.32	0.38	0.45	Watts	Saving realized moving from PH15 to LPM20, single core	(4)(5)

Notes:
1. Power for V_{DD} only.
2. Typical power assumes Dhrystone running (PH00 state) with activity factor of 70%.
3. Typical power based on nominal process distribution for this device.
4. PH10, PH15, LPM20 power savings with 1 core. Maximum savings would be N times, where N is the number of used cores.
5. LPM20 has all platform clocks disabled.

3.5.1 I/O DC power supply recommendation

This table provides the estimated I/O power numbers for each block: DDR, PCI Express, eLBC, eTSEC, SGMII, eSDHC, USB, eSPI, DUART, IIC, DIU, SATA and GPIO. Note that these numbers are based on design estimates only.

Table 3-10. I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
DDR3L	1600MT/s data rate	G1VDD(1.35V)	860	1760	mW	(1)(2)(5)
PCI Express	1x, 2.5 GT/s	X1VDD(1.35V)	50	62	mW	(1)(3)(6)
	2x, 2.5 GT/s		81	94		
	4x, 2.5 GT/s		145	158		
	8x, 2.5 GT/s		274	287		
	1x, 5 GT/s		50	70		
	2x, 5 GT/s		90	100		
	4x, 5 GT/s		150	160		
	8x, 5 GT/s		280	290		
SGMII	1x, 1.25 G-baud	X1VDD(1.35V)	50	60	mW	(1)(3)(6)
	2x, 1.25 G-baud		70	90		
	4x, 1.25 G-baud		130	140		
SGMII	1x, 5 G-baud	X1VDD(1.35V)	50	70	mW	(1)(3)(6)
	2x, 5 G-baud		90	100		
SATA	1x, 3.0 Gbps	X1VDD(1.35V)	50	60	mW	(1)(3)(6)
	2x, 3.0 Gbps		70	80		
IFC	16-bit, 100MHz	OVDD(1.8V)	35	61	mW	(1)(2)(6)
EC1	RGMII	L1VDD(2.5V)	155	220	mW	(1)(2)(6)
	RGMII	L1VDD(1.8V)	115	180	mW	(1)(2)(6)

Table 3-10. I/O power supply estimated values (Continued)

Interface	Parameter	Symbol	Typical	Maximum	Unit	Note
	MII	L1VDD(3.3V)	155	220	mW	(1)(2)(6)
EC2	RGMII	LVDD(2.5V)	155	220	mW	(1)(2)(6)
	RGMII	LVDD(1.8V)	115	180		
eSDHC		EVDD(3.3V)	11	17	mW	(1)(2)(6)
		EVDD(1.8V)	7	10		
USB1, USB2		USB_HVDD(3.3V)	40	60	mW	(1)(2)(6)
		USB_OVDD(1.8V)	100	110		
eSPI		CVDD(3.3V)	14	22	mW	(1)(2)(6)
		CVDD(1.8V)	11	16		
DIU		DVDD(3.3V)	70	90	mW	(1)(2)(6)
QE		DVDD(3.3V)	15	21	mW	(1)(2)(6)
		DVDD(2.5V)	11	17		
DDR3L Termination		VTT (G1VDD/2)	±200	±400	mW	(7)
I2C		DVDD(3.3V)	14	22	mW	(1)(2)(6)
		DVDD(2.5V)	10	16		
		DVDD(1.8V)	8	13		
DUART		DVDD(3.3V)	14	22	mW	(1)(2)(4)(6)
		DVDD(2.5V)	10	15		
		DVDD(1.8V)	8	12		
TDM		DVDD(3.3V)	10	14	mW	(1)(2)(6)
IEEE1588		LVDD(2.5V)	16	21	mW	(1)(2)(6)
GPIO	x8	3.3V	5	8	mW	(1)(2)(6)
	x8	2.5V	4	7		
	x8	1.8V	3	5		
System Control		O1VDD(1.8V)	45	70	mW	(1)(2)(6)
PLL core and system		AVDD_CGA1 (1.8V)	20	20	mW	(1)(2)(6)
		AVDD_CGA2 (1.8V)				
		AVDD_PLAT(1.8V)				
PLL DDR		AVDD_D1(1.8V)	30	40	mW	(1)(2)(6)
PLL SerDes		AVDD_SD1_PLL1, AVDD_SD1_PLL2(1.35V)	50	50	mW	(1)(2)(6)
PROG_SFP		PROG_SFP (1.8V)	173		mW	–
TH_VDD		TH_VDD (1.8V)	1		mW	–

Notes:
1. The typical values are estimates based on simulations 65ºC junction temperature.
2. Assuming 15 pF total capacitance load per pin.
3. The total power numbers of X1VDD is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the X1VDD power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.
4. GPIO are supported on OV_{DD}, $O1V_{DD}$, $L1V_{DD}$, LV_{DD}, DV_{DD}, CV_{DD} and EV_{DD} power rails.

5. Typical DDR power numbers are based on 40% utilization of the DDR, maximum DDR power numbers are based on 100% utilization of the DDR.
6. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case.The maximum values are estimated and they are based on simulations at 105ºC junction temperature.
7. Source and sink value.

3.5.2 DDR3L power consumption

This table provides the estimated power numbers for the 1GB of DDR3L embedded in the QT1040.

Table 3-11. DDR3L power consumption

Symbol	Parameter/Condition	DDR3L- 1600 Max.	
IDD0	Operating Current 0 -> One Bank Activate-> Precharge	473	mW
IDD1	Operating Current 1 -> One Bank Activate-> Read-> Precharge	608	mW
IDD2P0	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	81	mW
IDD2P1	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	216	mW
IDD2PQ	Precharge Quiet Standby Current	270	mW
IDD2N	Precharge Standby Current	297	mW
IDD3P	Active Power-Down Current Always Fast Exit	304	mW
IDD3N	Active Standby Current	351	mW
IDD4R	Operating Current Burst Read	1080	mW
IDD4W	Operating Current Burst Write	1215	mW
IDD5B	Burst Refresh Current	1080	mW
IDD6	Self-Refresh Current Normal Temperature Range (0-85°C)	81	mW
IDD6ET	Self-Refresh Current: extended temperature range	101	mW
IDD7	All Bank Interleave Read Current	1856	mW

3.6 Input clocks

3.6.1 System clock (SYSCLK) timing specifications

This section provides the system clock DC and AC timing specifications.

3.6.1.1 System clock DC timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 3-12. SYSCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	–	–	V	(1)
Input low voltage	V_{IL}	–	–	0.6	V	(1)
Input capacitance	C_{IN}	–	7	12	pF	–
Input current ($O1V_{IN}$ = 0V or $O1V_{IN}$ = $O1V_{DD}$)	I_{IN}	–	–	± 50	µA	(2)

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max $O1V_{IN}$ values found in Table 3-2.
2. The symbol OV_{IN}, in this case, represents the $O1V_{IN}$ symbol referenced in Recommended operating conditions.
3. At recommended operating conditions with $O1V_{DD}$ = 1.8V, see Table 3-2.

3.6.1.2 System clock AC timing specifications

This table provides the system clock (SYSCLK) AC timing specifications.

Table 3-13. SYSCLK AC timing specifications[1]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	64.0	–	133.3	MHz	(2)(5)
SYSCLK cycle time	t_{SYSCLK}	7.5	–	15.6	ns	(1)(2)
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	–	60	%	(2)
SYSCLK slew rate	–	1	–	4	V/ns	(3)
SYSCLK peak period jitter	–	–	–	± 150	ps	–
SYSCLK jitter phase noise at –56 dBc	–	–	–	500	KHz	(4)
AC Input Swing Limits at 1.8V $O1V_{DD}$	ΔV_{AC}	1.08	–	1.8	V	–

Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency does not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $O1V_{DD}/2$.
3. Slew rate as measured from 0.35 × $O1V_{DD}$ to 0.65 × $O1V_{DD}$.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with $O1V_{DD}$ = 1.8V, see Table 3-2.

3.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in Table 3-13 considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in Table 3-13 are observed.

Table 3-14. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	–	60	kHz	–
Frequency spread	–	1.0	%	(1)(2)

Notes:
1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 3-13.
2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.
3. At recommended operating conditions with $O1V_{DD}$ = 1.8V, see Table 3-2.

CAUTION

The processor's minimum and maximum SYSCLK and core/ platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

3.6.3 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

3.6.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC specifications.

Table 3-15. EC*n*_GTX_CLK125 DC electrical characteristics (L1VDD/LVDD=1.8V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * VDD	–	–	V	(2)(4)
Input low voltage	V_{IL}	–	–	0.2 * VDD	V	(2)(4)
Input capacitance	C_{IN}	–	–	6	pF	–
Input current (V_{IN} = 0V or V_{IN} = $L1V_{DD}$)/LV_{DD})	I_{IN}	–	–	± 50	µA	(3)

Notes:
1. At recommended operating conditions with $L1V_{DD}/LV_{DD}$ = 1.8V
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 3-2.
3. The symbol V_{IN}, in this case, represents the $L1V_{IN}/LV_{IN}$ symbol referenced in Recommended operating conditions.
4. ECn_GTX_CLK125 is powered by $L1V_{DD}$ and LV_{DD}. VDD should be replaced by the respective IO power supply.

This table provides the Ethernet gigabit reference clock DC specifications.

Table 3-16. EC*n*_GTX_CLK125 DC electrical characteristics ((L1VDD/LVDD=2.5V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * VDD	–	–	V	(2)(4)
Input low voltage	V_{IL}	–	–	0.2 * VDD	V	(2)(4)
Input capacitance	C_{IN}	–	–	6	pF	–
Input current (V_{IN} = 0V or V_{IN} = $L1V_{DD}$)/LV_{DD})	I_{IN}	–	–	± 50	µA	(3)

Notes:
1. At recommended operating conditions with $L1V_{DD}/LV_{DD}$ = 2.5V
2. The min V_{IL} and max V_{IH} values are based on the respective min and max v_{IN} values found in Table 3-2.
3. The symbol v_{IN}, in this case, represents the $L1v_{IN}/Lv_{IN}$ symbol referenced in Recommended operating conditions.
4. ECn_GTX_CLK125 is powered by $L1V_{DD}$ and LV_{DD}. VDD should be replaced by the respective IO power supply.

This table provides the Ethernet gigabit reference clocks AC timing specifications.

Table 3-17. EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	t_{G125}	125 – 100 ppm	125	125 + 100 ppm	MHz	–
EC*n*_GTX_CLK125 cycle time	t_{G125}	–	8	–	ns	–
EC*n*_GTX_CLK125 rise and fall time $L1/LV_{DD}$ = 1.8V $L1/LV_{DD}$ = 2.5V	t_{G125R}/t_{G125F}	–	–	0.54 0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base–T for RGMII	t_{G125H}/t_{G125}	40	–	60	%	3
EC*n*_GTX_CLK125 jitter	–	–	–	± 150	ps	3

Notes:
1. At recommended operating conditions with $L1/LV_{DD}$ = 1.8V ± 90mV / 2.5V ± 125 mV.
2. Rise and fall times for EC*n*_GTX_CLK125 are measured from 0.5 and 2.0V for $L1/LV_{DD}$ = 2.5V.
3. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for 10Base-T and 100Base-T reference clock.

3.6.5 DDR clock timing

This section provides the DDR clock DC and AC timing specifications.

3.6.5.1 DDR clock DC timing specifications

This table provides the DDR clock (DDRCLK) DC specifications.

Table 3-18. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	–	–	V	1
Input low voltage	V_{IL}	–	–	0.6	V	1
Input capacitance	C_{IN}	–	7	12	pF	–
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	–	–	± 50	µA	2

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3-2.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3-2.

3.6.5.2 DDR clock AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 3-19. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	64.0	–	133.3	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	7.5	–	15.6	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	–	60	%	2
DDRCLK slew rate	–	1	–	4	V/ns	3
DDRCLK peak period jitter	–	–	–	± 150	ps	–
DDRCLK jitter phase noise at –56 dBc	–	–	–	500	KHz	4
AC Input Swing Limits at 1.8V OV_{DD}	ΔV_{AC}	1.08	–	1.8	V	–

Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequency does not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from 0.35 × OV_{DD} to 0.65 × OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3-2.

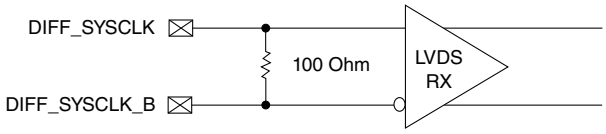
3.6.6 Differential System clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

"Single Oscillator Source" clocking mode requires single onboard oscillator to provide reference clock input to Differential System clock pair (DIFF_SYSCLK/ DIFF_SYSCLK_B).

This Differential clock pair can be configured to provide clock to Core, Platform, DDR and USB PLL's

This figure shows a receiver reference diagram of the Differential System clock.

Figure 3-4. LVDS receiver



This section provides the differential system clock DC and AC timing specifications.

3.6.6.1 Differential System clock DC timing specifications

For DC timing specification, see DC-level requirement for SerDes reference clocks

The Differential System clock receivers core power supply voltage requirements ($O1V_{DD}$) are as specified in Recommended operating conditions.

The Differential system clock can also be single-ended. For this DIFF_SYSCLK_B should be connected to $O1V_{DD}/2$.

3.6.6.2 Differential System clock AC timing specifications

Differential System clock (DIFF_SYSCLK/DIFF_SYSCLK_B) input pair supports input clock frequency of 100MHz

For AC timing specification, see AC requirements for SerDes reference clocks

Spread Spectrum clocking is not supported on Differential System clock pair input.

3.6.7 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, Ethernet management, eSDHC, IFC, see the specific interface section.

3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

Table 3-20. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1	–	ms	(1)
Required input assertion time of HRESET_B	32	–	SYSCLKs	(2)(3)
Maximum rise/fall time of HRESET_B	–	10	SYSCLK	(4)
Maximum rise/fall time of PORESET_B	–	1	SYSCLK	(4)
PLL input setup time with stable SYSCLK before HRESET_B negation	100	–	µs	–
Input setup time for POR configs with respect to negation of PORESET_B	4	–	SYSCLKs	(2)
Input hold time for all POR configs with respect to negation of PORESET_B	2	–	SYSCLKs	(2)
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	–	5	SYSCLKs	(2)

Notes:
1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The
4. device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in section "Power-On Reset Sequence" in the chip reference manual.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

This table provides the PLL lock times.

Table 3-21. PLL lock times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times (Core, platform, DDR only)	–	100	µs	–

3.8 DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3L SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.35V when interfacing to DDR3L SDRAM.

Note: In the QT1040, DDR3L signals are not available at package boundary for users (except RESET#)

3.8.1 DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 3-22. DDR3L SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.35V)[(1)(9)]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$D1\_MV_{REF}$	0.49 × $G1V_{DD}$	0.51 × $G1V_{DD}$	V	(2)(3)(4)
Input high voltage	V_{IH}	$D1\_MV_{REF}$ + 0.090	$G1V_{DD}$	V	(5)
Input low voltage	V_{IL}	GND	$D1\_MV_{REF}$ – 0.090	V	(5)
I/O leakage current	I_{OZ}	–100	100	µA	(6)
Output high current (V_{OUT} = 0.641V)	I_{OH}	–	–23.3	mA	(7)(8)
Output low current (V_{OUT} =0.641V)	I_{OL}	23.3	–	mA	(7)(8)

Notes:
1. $G1V_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times. The voltage supply of DRAM and memory controller may or may not be from the same source.
2. $D1\_MV_{REF}$ is expected to be equal to 0.5 × $G1V_{DD}$ and to track $G1V_{DD}$ DC variations as measured at the receiver. Peak- to-peak noise on $D1\_MV_{REF}$ may not exceed the $D1\_MV_{REF}$ DC level by more than ±1% of $G1V_{DD}$ (that is, ±13.5mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $D1\_MV_{REF}$ with a min value of $D1\_MV_{REF}$ - 0.04 and a max value of $D1\_MV_{REF}$ + 0.04. V_{TT} should track variations in the DC level of $D1\_MV_{REF}$.
4. The voltage regulator for $D1\_MV_{REF}$ must meet the specifications stated in Table 3-23.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0V = V_{OUT} = $G1V_{DD}$.
7. See the IBIS model for the complete output IV curve characteristics.
8. I_{OH} and I_{OL} are measured at $G1V_{DD}$ = 1.283V.
9. For recommended operating conditions, see Table 3-2.

This table provides the current draw characteristics for $D1\_MV_{REF}$.

Table 3-23. Current draw characteristics for D1_MV [1]

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3L SDRAM for $D1\_MV_{REF}$	I_{D1_MVREF}	–	500	µA	–

Note: 1. For recommended operating conditions, see Table 3-2.

3.8.2 DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3L memories. Note that the required $G1V_{DD}$(typ) voltage is 1.35V when interfacing to DDR3L.

3.8.2.1 DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 3-24. DDR3L SDRAM interface input AC timing specifications[1]

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	–	D1_MVREF- 0.135	V	–
	= 1200 MT/s data rate			D1_MVREF- 0.160		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	D1_MVREF+ 0.135	–	V	–
	= 1200 MT/s data rate		D1_MVREF+ 0.160			

Note: 1. For recommended operating conditions, see Table 3-2.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

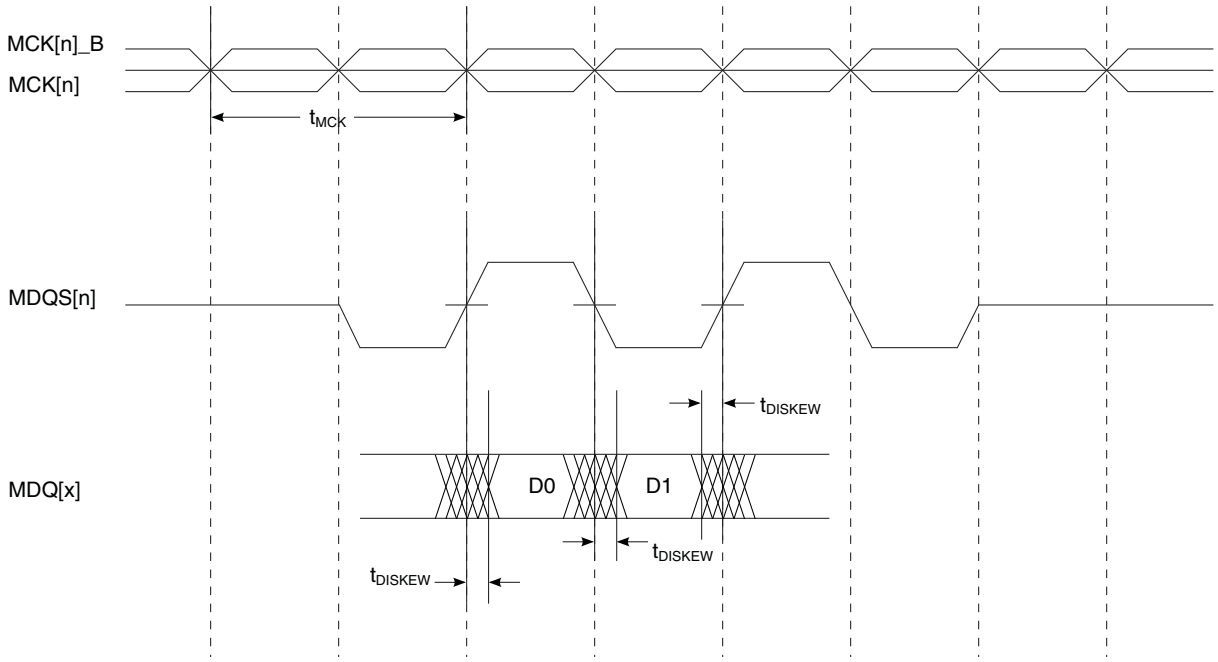
Table 3-25. DDR3L SDRAM interface input AC timing specifications(3)

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}			ps	
1600 MT/s data rate		–112	112		(1)
1300 MT/s data rate		–125	125		(1)
1200 MT/s data rate		–142	142		(1)(4)
1000 MT/s data rate		–170	170		(1)(4)
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}			ps	
1600 MT/s data rate		–200	200		(2)
1300 MT/s data rate		–250	250		(2)
1200 MT/s data rate		–275	275		(2)(4)
1000 MT/s data rate		–300	300		(2)(4)

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. For recommended operating conditions, see Table 3-2.
4. DDR3L only

This figure shows the DDR3L SDRAM interface input timing diagram.

Figure 3-5. DDR3L SDRAM Interface Input Timing Diagram



3.8.2.2 *DDR3L SDRAM interface output AC timing specifications*

This table contains the output AC timing targets for the DDR3L SDRAM interface.

Table 3-26. DDR3L SDRAM interface output AC timing specifications[8]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1250	1876	ps	(2)
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ps	
1600 MT/s data rate		495	–		(3)
1300 MT/s data rate		606	–		(3)
1200 MT/s data rate		675	–		(3)(6)
1000 MT/s data rate		744	–		(3)(6)
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ps	
1600 MT/s data rate		495	–		(3)
1300 MT/s data rate		606	–		(3)
1200 MT/s data rate		675	–		(3)(6)
1000 MT/s data rate		744	–		(3)(6)
MCK to MDQS Skew	t_{DDKHMH}			ps	(4)
> 1000 MT/s data rate, = 1600 MT/s data rate		–245	245		(7)
MDQ/MECC/MDM output Data eye	$t_{DDKXDEYE}$			ps	
1600 MT/s data rate		400	–		(5)
1300 MT/s data rate		500	–		(5)
1200 MT/s data rate		550	–		(5)(6)
1000 MT/s data rate		600	–		(5)(6)
MDQS preamble	t_{DDKHMP}	$900 \times t_{MCK}$	–	ps	–
MDQS postamble	t_{DDKHME}	$400 \times t_{MCK}$	$600 \times t_{MCK}$	ps	–

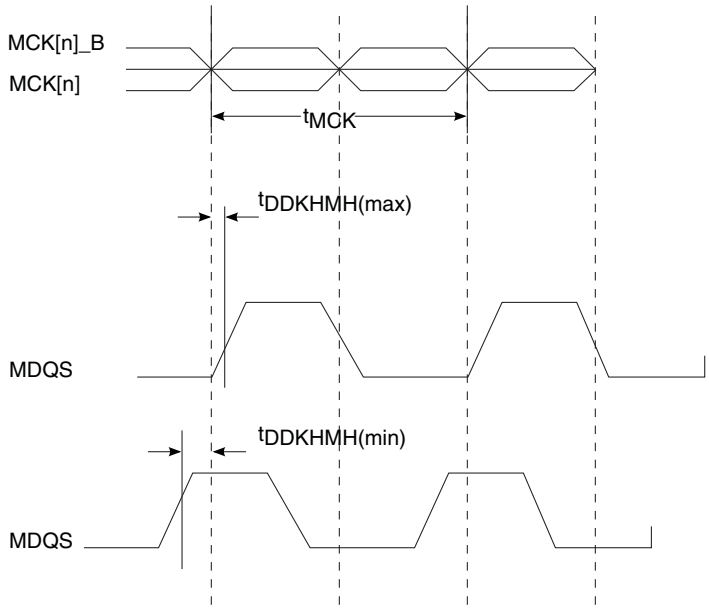
Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.
5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.
6. DDR3L only

7. Note that it is required to program the start value of the MDQS adjust for write leveling.
8. For recommended operating conditions, see Table 3-2.

NOTE
For the ADDR/CMD/CNTL setup and hold specifications in Table 3-26, it is assumed that the clock control register is set to adjust the memory clocks by ¾ applied cycle.

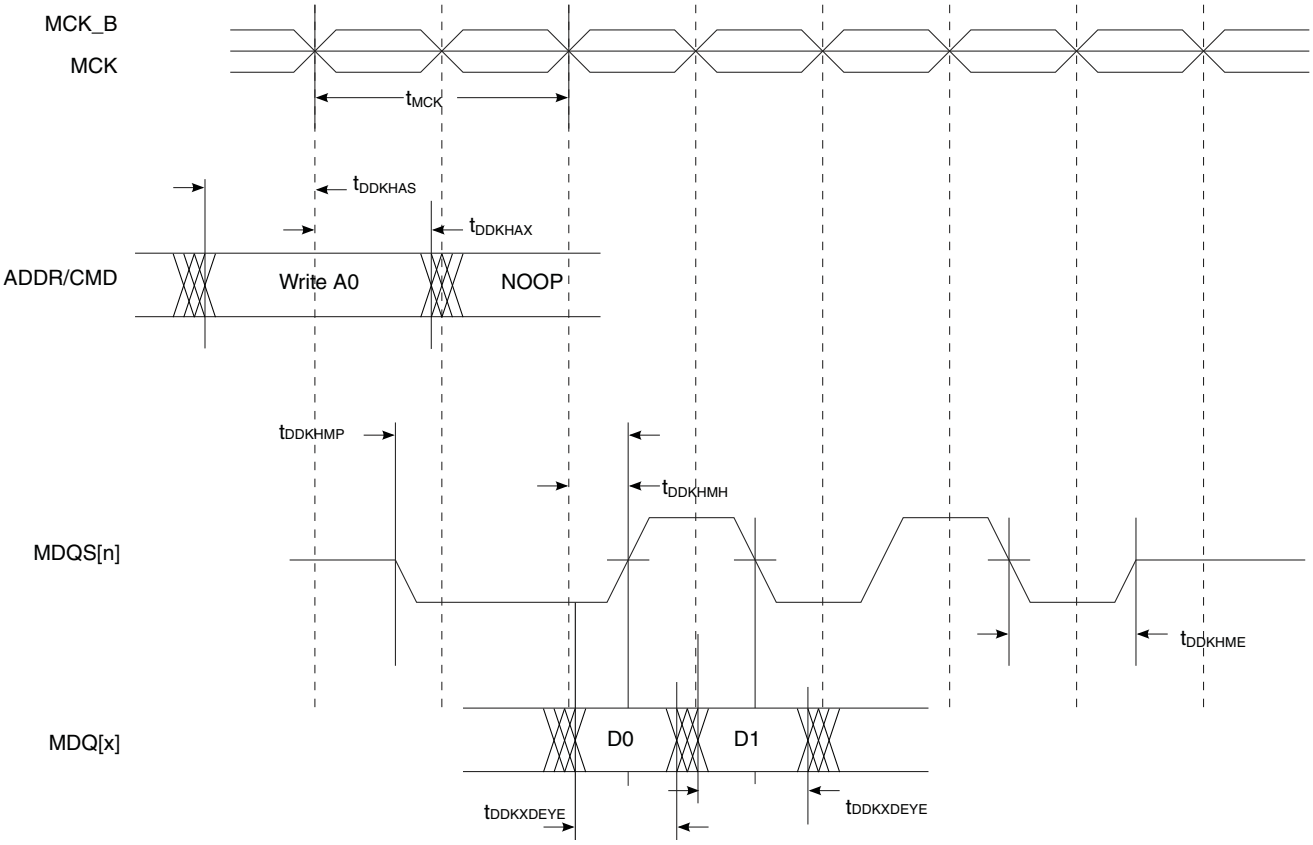
This figure shows the DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

Figure 3-6. t_{DDKHMH} timing diagram



This figure shows the DDR3L SDRAM output timing diagram.

Figure 3-7. DDR3L output timing diagram



3.9 eSPI interface

This section describes the DC and AC electrical specifications for the eSPI interface.

3.9.1 eSPI DC electrical characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8V.

Table 3-27. eSPI DC electrical characteristics (1.8V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * CVDD	–	V	2
Input low voltage	V_{IL}	–	0.2 * CVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = CV_{DD})	I_{IN}	–	±50	µA	3
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. For recommended operating conditions, see Table 3-2.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3-2.
3. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Recommended operating conditions.

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 3.3V.

Table 3-28. eSPI DC electrical characteristics (3.3V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * CVDD	–	V	2
Input low voltage	V_{IL}	–	0.2 * CVDD	V	2
Input current (V_{IN} = 0V or V_{IN} = CV_{DD})	I_{IN}	–	±50	µA	–
Output high voltage (CV_{DD} = min, I_{OH} = –2.0 mA)	V_{OH}	2.4	–	V	–
Output low voltage (CV_{DD} = min, I_{OL} = 2.0 mA)	V_{OL}	–	0.4	V	–

Notes: 1. For recommended operating conditions, see Table 3-2.

2. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3-2.

3.9.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 3-29. eSPI AC timing specifications(3)

Parameter/Condition	Symbol(2)	Min	Max	Unit	Notes
SPI_MOSI output-Master data (internal clock) hold time	t_{NIKHOX}	–0.49 + ($t_{PLATFORM\_CLK/2}$ * SPMODE[HO_ADJ])	–	ns	(1)(2)
SPI_MOSI output-Master data (internal clock) delay	t_{NIKHOV}	–	0.89 + ($t_{PLATFORM\_CLK/2}$ * SPMODE[HO_ADJ])	ns	(1)(2)
SPI_CS outputs-Master data (internal clock) hold time	$t_{NIKHOX2}$	–100	–	ps	(1)
SPI_CS outputs-Master data (internal clock) delay	$t_{NIKHOV2}$	–	6.0	ns	(1)
SPI inputs-Master data (internal clock) input setup time	t_{NIIVKH}	6.6	–	ns	–
SPI inputs-Master data (internal clock) input hold time	t_{NIIXKH}	0	–	ns	–
Clock-high time	t_{NIKCKH}	4	–	ns	
Clock–low time	t_{NIKCKL}	4	–	ns	–

Notes: 1. See the chip reference manual for details about the SPMODE register.

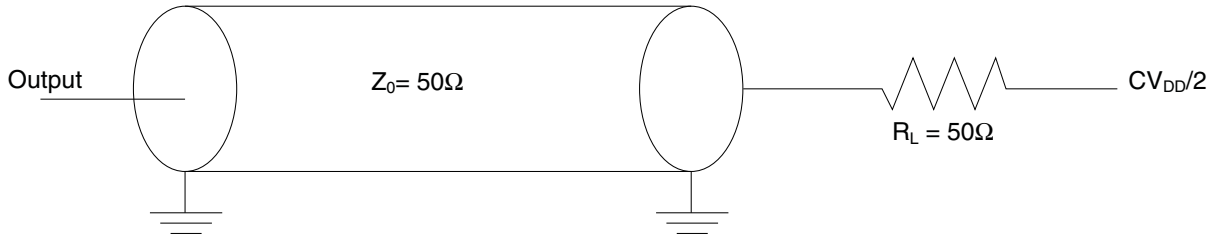
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

3. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

4. Refer AN4375 to calculate maximum achievable eSPI interface frequency on a system.

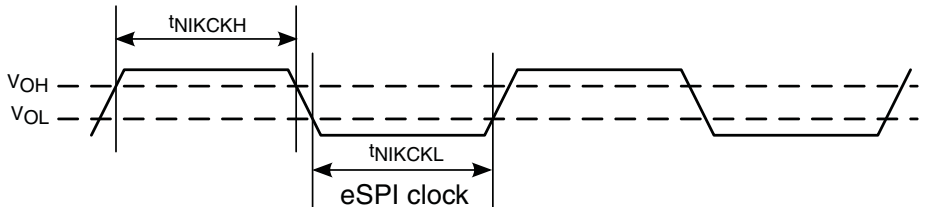
This figure provides the AC test load for the eSPI.

Figure 3-8. eSPI AC test load



This figure provides the eSPI clock output timing diagram.

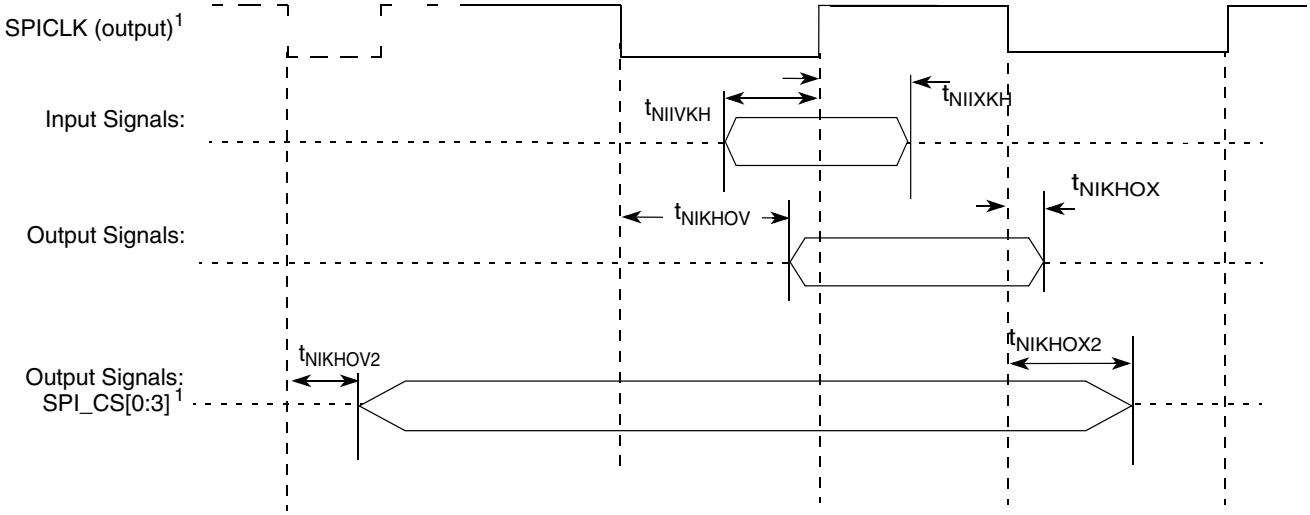
Figure 3-9. eSPI clock output timing diagram



Note: 1. SPICLK appears on the interface only after CS assertion.

This figure represents the AC timing from Table 3-29 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

Figure 3-10. eSPI AC timing in master mode (internal clock) diagram



3.10 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.10.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 3.3V.

Table 3-30. DUART DC electrical characteristics (3.3V)(3)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7*VDD	–	V	(1)(4)
Input low voltage	V_{IL}	–	0.2*VDD	V	(1)(4)
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	(3)
Output high voltage	V_{OH}	2.4	–	V	–
(DV_{DD} = min, I_{OH} = –2.0 mA)					
Output low voltage	V_{OL}	–	0.4	V	–
(DV_{DD} = min, I_{OL} = 2.0 mA)					

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. VDD should be replaced by the respective IO power supply.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 2.5V.

Table 3-31. DUART DC electrical characteristics(2.5V)(3)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7*VDD	–	V	(1)(4)
Input low voltage	V_{IL}	–	0.2*VDD	V	(1)(4)
Input current (DV_{IN} = 0V or DV_{IN}= DV_{DD})	I_{IN}	–	±50	µA	(2)
Output high voltage (DV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. VDD should be replaced by the respective IO power supply.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8V.

Table 3-32. DUART DC electrical characteristics(1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7*VDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2*VDD	V	1, 4
Input current (DV_{IN} = 0V or DV_{IN}= DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (DV_{DD} = min, I_{OL}= 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol DV_{IN} represents the input voltage of the supply.It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. VDD should be replaced by the respective IO power supply.

3.10.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 3-33. DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 × 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 × 16)	baud	1, 2

Notes:
1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3.11 Ethernet interface, Ethernet management interface, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interface.

3.11.1 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 3-11, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 3-63.

3.11.1.1 SGMII clocking requirements for SD1_REF_CLKn_P and SD1_REF_CLKn_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.
For more information on these specifications, see SerDes reference clocks.

3.11.1.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.11.1.2.1 SGMII transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N)as shown in Figure 3-12.

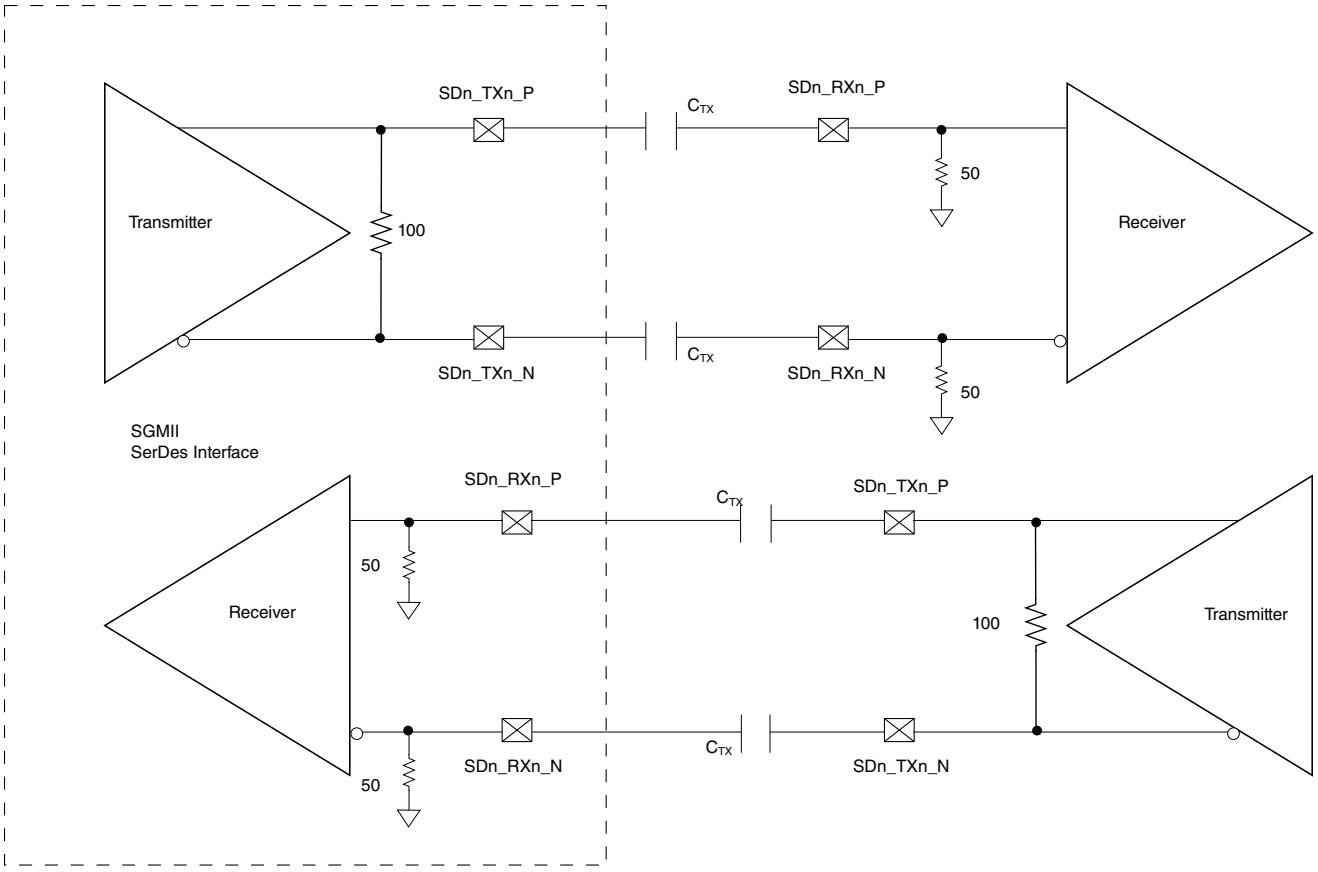
Table 3-34. SGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	–	–	1.5 × I V_{OD} I $_{-max}$	mV	[1]
Output low voltage	V_{OL}	I V_{OD} I $_{-min}$/2	–	–	mV	[1]
Output differential voltage[2][3][5] (XV_{DD-Typ} at 1.35V)	I V_{OD} I	320	500.0	725.0	mV	TECR0[AMP_RED]=0b00 0000
		293.8	459.0	665.6		TECR0[AMP_RED]=0b00 0001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b00 0011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b00 0010
		213.1	333.0	482.9		TECR0[AMP_RED]=0b00 0110
		186.9	292.0	423.4		TECR0[AMP_RED]=0b00 0111
		160.0	250.0	362.5		TECR0[AMP_RED]=0b01 0000
Output impedance (differential)	R_o	80	100	120	Ω	–

Notes:
1. This does not align to DC-coupled SGMII.
2. I V_{OD} I = I $V_{SD\_TXn\_P}$ – $V_{SD\_TXn\_N}$ I. I V_{OD} I is also referred to as output differential peak voltage. $V_{TX-DIFFp-p}$ = 2 × I V_{OD} I.
3. The I V_{OD} I value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.
4. For recommended operating conditions, see Table 3-2.
5. Example amplitude reduction setting for SGMII on SerDes1 lane E: SRDS1LN4TECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

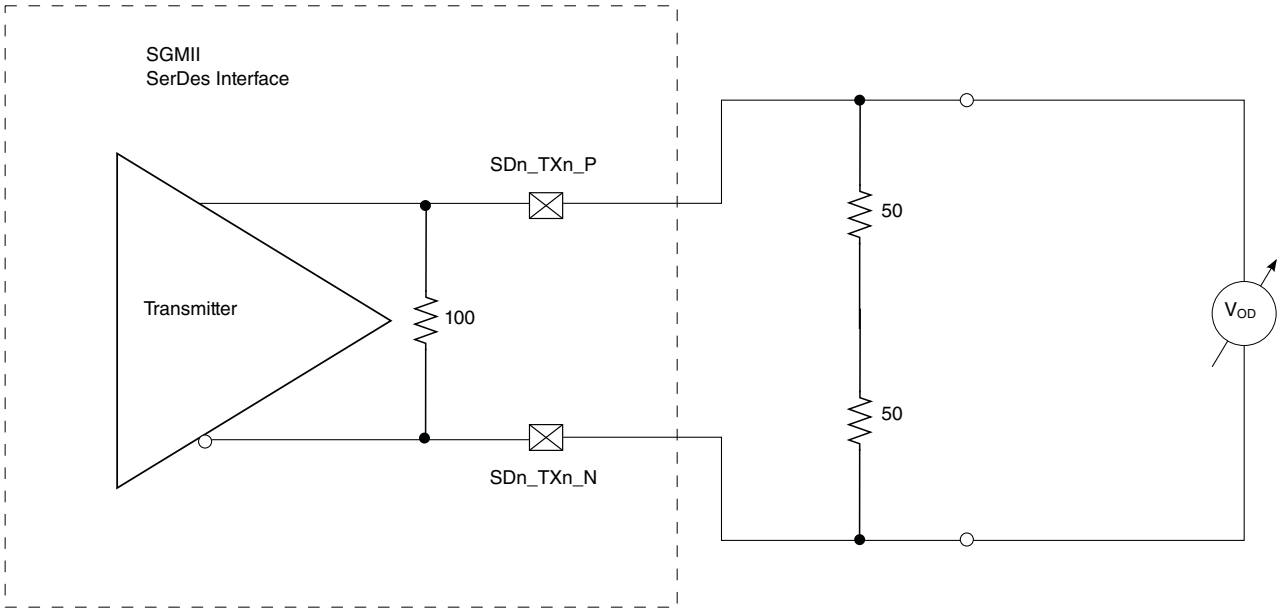
This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

Figure 3-11. 4-wire AC-coupled SGMII serial link connection example



This figure shows the SGMII transmitter DC measurement circuit.

Figure 3-12. SGMII transmitter DC measurement circuit



3.11.1.2.2 SGMII DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 3-35. SGMII DC receiver electrical characteristics (S1VDD = 1.0V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		–	N/A			–	(1)
Input differential voltage	REIDL_TH = 001	$V_{RX\_DIFFp-p}$	100	–	1200	mV	(2)(5)
	REIDL_TH = 100		175	–			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	–	100	mV	(3)(5)
	REIDL_TH = 100		65	–	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	–	120	Ω	–

Notes:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.
4. For recommended operating conditions, see Table 3-2.
5. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.

3.11.1.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

3.11.1.3.1 SGMII transmit AC timing specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 3-36. SGMII transmit AC timing specifications4

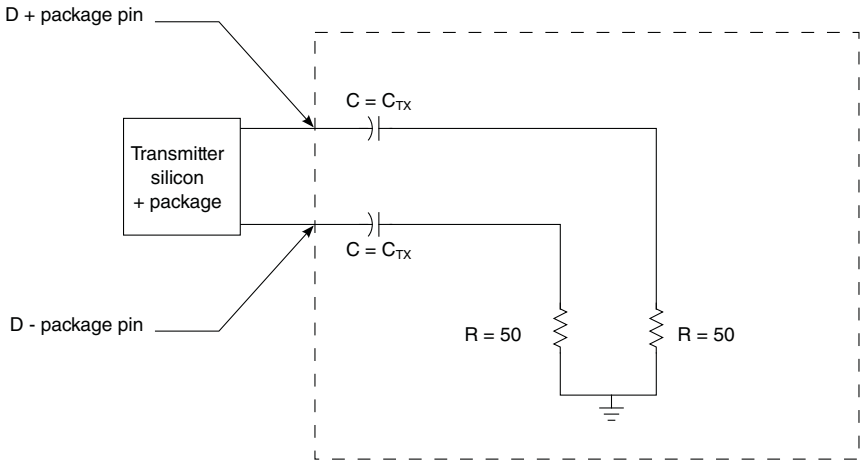
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	–	–	0.17	UI p-p	–
Total jitter	JT	–	–	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	–	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 3-14 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. For recommended operating conditions, see Table 3-2.

3.11.1.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N) or at the receiver inputs (SD1_RX*n*_P and SD1_RX*n*_N) respectively, as depicted in this figure.

Figure 3-13. SGMII AC test/measurement load



3.11.1.3.3 SGMII receiver AC timing Specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

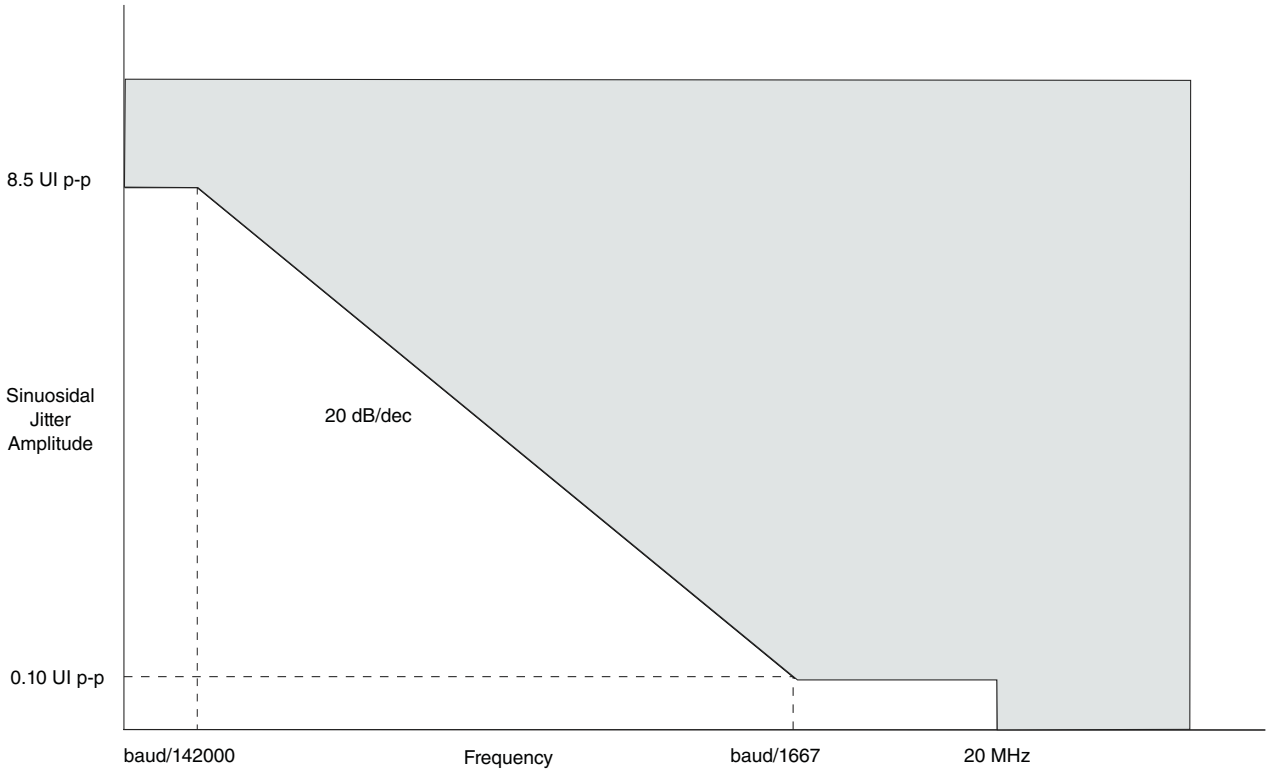
Table 3-37. SGMII Receive AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	–	–	0.37	UI p-p	(1)
Combined deterministic and random jitter tolerance	J_{DR}	–	–	0.55	UI p-p	(1)
Total jitter tolerance	J_T	–	–	0.65	UI p-p	(1)(2)
Bit error ratio	BER	–	–	10^{-12}	–	–
Unit Interval: 1.25 GBaud (SGMII)	UI	800 – 100 ppm	800	800 + 100 ppm	ps	(1)

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 3-14. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. For recommended operating conditions, see Table 3-2.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

Figure 3-14. Single-frequency sinusoidal jitter limits



3.11.2 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.11.2.1 QSGMII clocking requirements for SDn_REF_CLKn and SDn_REF_CLKn_B

For more information on these specifications, see SerDes reference clocks.

3.11.2.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.11.2.2.1 QSGMII transmitter DC specifications

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B).

Table 3-38. QSGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	–	900	mV	–
Differential resistance	T_{RD}	80	100	120	Ω	–

Note: 1. For recommended operating conditions, see Table 3-2.

3.11.2.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 3-39. QSGMII receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	–	900	mV	–
Differential resistance	R_{RDIN}	80	100	120	Ω	–

Note: 1. For recommended operating conditions, see Table 3-2.

3.11.2.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.11.2.3.1 QSGMII transmit AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 3-40. QSGMII transmit AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gb/s	–
Uncorrelated high probability jitter	T_{UHPJ}	–	–	0.15	UI p-p	–
Total jitter tolerance	J_T	–	–	0.30	UI p-p	–

Note: 1. For recommended operating conditions, see Table 3-2.

3.11.2.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

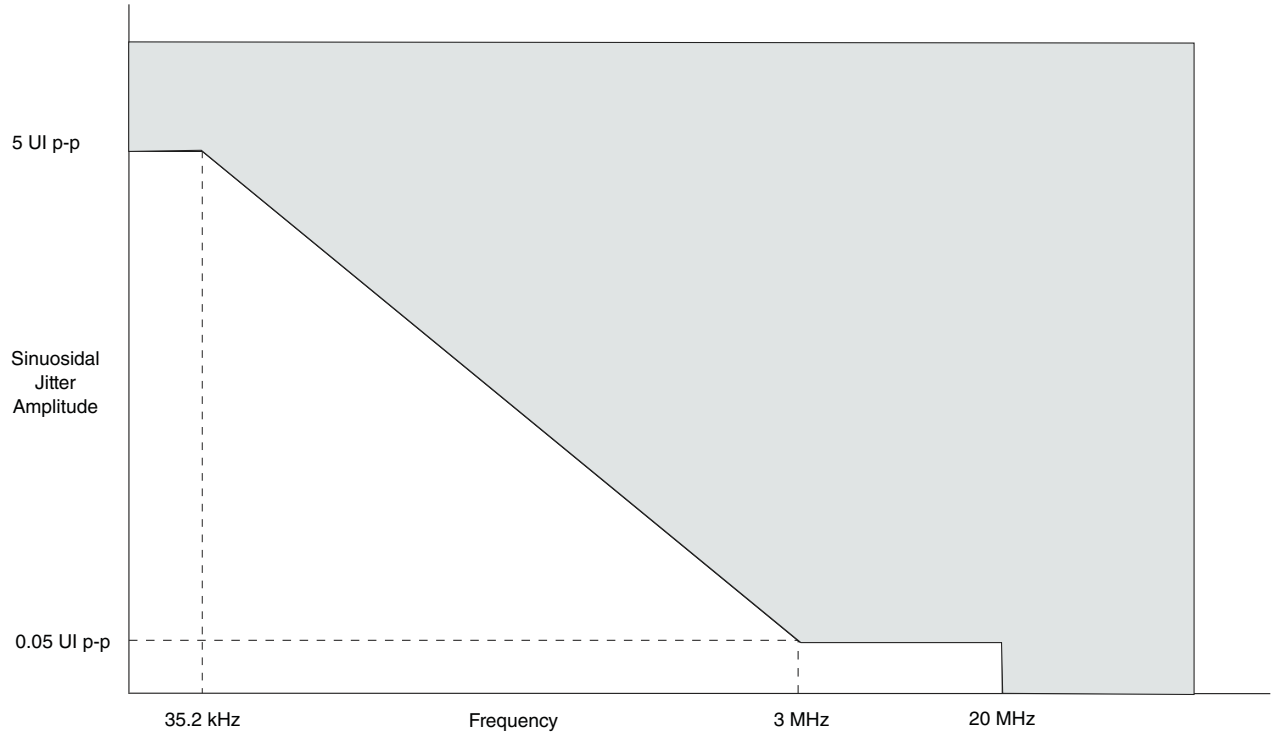
Table 3-41. QSGMII receive AC timing specifications[(2)]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gb/s	–
Uncorrelated bounded high probability jitter	R_{DJ}	–	–	0.15	UI p-p	–
Correlated bounded high probability jitter	R_{CBHPJ}	–	–	0.30	UI p-p	(1)
Bounded high probability jitter	R_{BHPJ}	–	–	0.45	UI p-p	–
Sinusoidal jitter, maximum	R_{SJ-max}	–	–	5.00	UI p-p	–
Sinusoidal jitter, high frequency	R_{SJ-hf}	–	–	0.05	UI p-p	–
Total jitter (does not include sinusoidal jitter)	R_{Tj}	–	–	0.60	UI p-p	–

Notes: 1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 3-2.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

Figure 3-15. QSGMII single-frequency sinusoidal jitter limits



3.11.3 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC- coupled operation is supported.

3.11.3.1 1000Base-KX DC electrical characteristics

3.11.3.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TXn_P and SD1_TXn_N).

Table 3-42. 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	–	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	–

Notes: 1. SRDSxLNmTECR0[AMP_RED]=00_0000.

2. For recommended operating conditions, see Table 3-2.

3.11.3.1.2 1000Base-KX Receiver DC Specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

Table 3-43. 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	–	–	1600	mV	1
Differential resistance	T_{RDIN}	80	–	120	ohm	–

Note: 1. For recommended operating conditions, see Table 3-2.

3.11.3.2 1000Base-KX AC electrical characteristics

3.11.3.2.1 1000Base-KX Transmitter AC Specifications

Table below provides the 1000Base-KX transmitter AC specification.

Table 3-44. 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	–
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	–	–	0.15	UI p-p	–
Deterministic Jitter	T_{DJ}	–	–	0.10	UI p-p	–
Total Jitter	T_{TJ}	–	–	0.25	UI p-p	1

Notes: 1. Total jitter is specified at a BER of 10^{-12}.
2. For recommended operating conditions, Table 3-2.

3.11.3.2.2 1000Base-KX Receiver AC Specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 3-45. 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	–
Random Jitter	R_{RJ}	–	–	0.15	UI p-p	1
Sinusoidal Jitter, maximum	R_{SJ-max}	–	–	0.10	UI p-p	2
Total Jitter	R_{TJ}	–	–	See Note 3	UI p-p	2

Notes: 1. Random jitter is specified at a BER of 10^{-12}.
2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
3. Per IEEE 802.3ap-clause 70.
4. The AC specifications do not include Refclk jitter.
5. For recommended operating conditions, Table 3-2.

3.11.4 RGMII electrical specifications

This section discusses the electrical characteristics for the RGMII interface.

3.11.4.1 RGMII DC electrical characteristics

This table shows the DC electrical characteristics for the RGMII interface.

Table 3-46. RGMII DC electrical characteristics(LV_{DD}, $L1V_{DD}$ = 2.5V)(4)

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	(1)
Input low voltage	V_{IL}	–	0.2 * LVDD	V	(1)
Input current (LV_{IN} = 0V or LV_{IN} = LV_{DD})	I_{IH}	–	±50	µA	(2)(3)
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	–	V	(3)
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.4	V	(3)

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} and $L1V_{IN}$ symbol referenced in Recommended operating conditions.
3. The symbol LV_{DD}, in this case, represents the LV_{DD} and $L1V_{DD}$ symbol referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 3-2.

This table provides the DC electrical characteristics for the RGMII interface at $L1V_{DD}/LV_{DD}$ = 1.8V.

Table 3-47. RGMII DC electrical characteristics(1.8V)(4)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	(1)
Input low voltage	V_{IL}	–	0.2 * LVDD	V	(1)
Input current (LV_{IN} = 0V or $L1V_{IN}$ = LV_{DD})	I_{IN}	–	±50	µA	(2)(3)
Output high voltage (LV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	(3)
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	(3)

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} values found in Table 3-2.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} and $L1V_{IN}$ symbol referenced in Recommended operating conditions.
3. The symbol LV_{DD}, in this case, represents the LV_{DD} and $L1V_{DD}$ symbol referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 3-2.

3.11.4.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

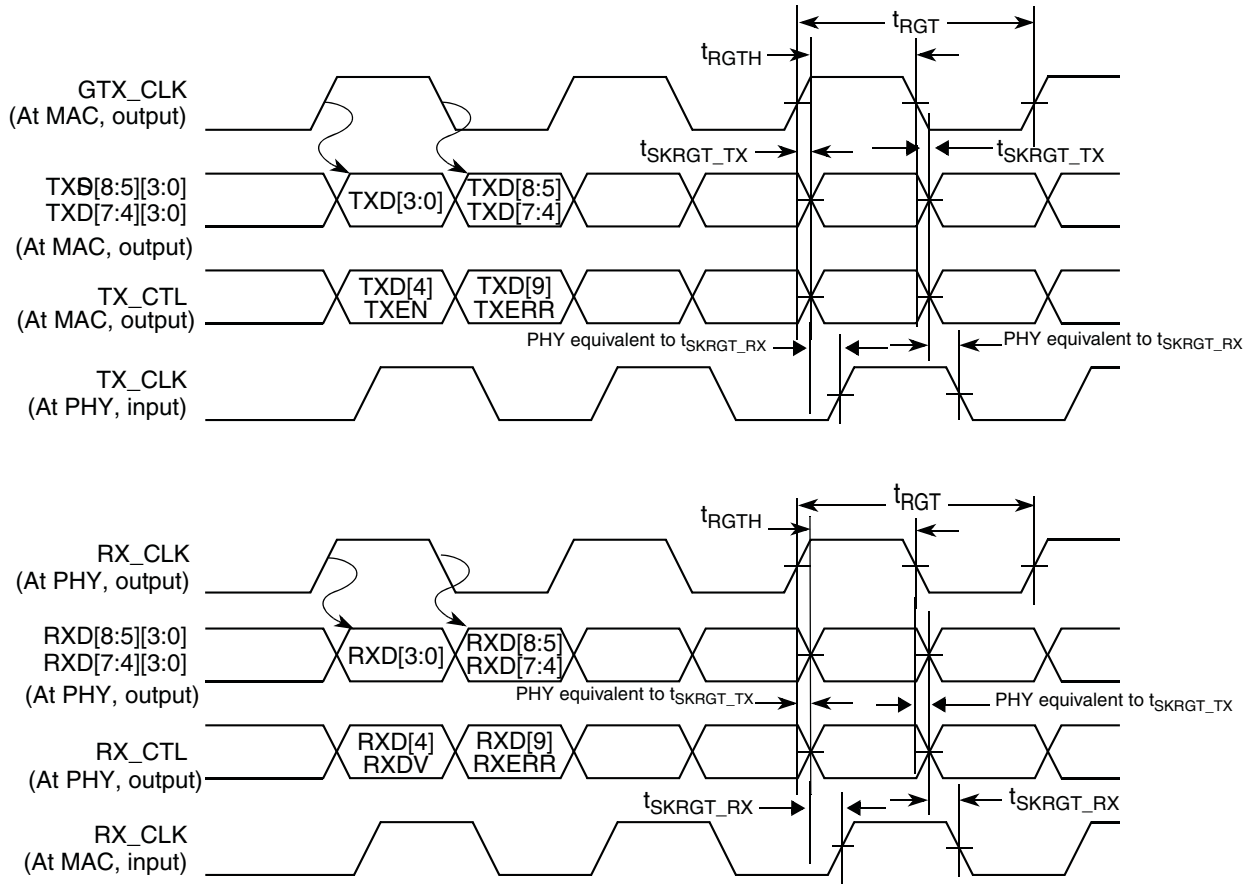
Table 3-48. RGMII AC timing specifications (LV_{DD} = 2.5 /1.8V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–620	0	520	ps	[7]
Data to clock input skew (at receiver)	t_{SKRGT_RX}	2.0	–	3.0	ns	[2]
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	[3]
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	[3][4]
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	–
Rise time (20%-80%) L1/LV_{DD} = 2.5V L1/LV_{DD} = 1.8V	t_{RGTR}	–	–	– 0.75 0.54	ns	[5][6]
Fall time (20%-80%) L1/LV_{DD} = 2.5V L1/LV_{DD} = 1.8V	t_{RGTF}	–	–	– 0.75 0.54	ns	[5][6]

Notes:
1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 2.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Applies to inputs and outputs.
6. System/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
7. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.
8. For recommended operating conditions, see Table 3-2.

This figure shows the RGMII AC timing and multiplexing diagrams.

Figure 3-16. RGMII AC timing and multiplexing diagrams



Warning

TELEDYNE e2v guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.11.5 MII electrical specifications

This section discusses the electrical characteristics for the MII interface.

3.11.5.1 MII DC electrical characteristics

This table shows the MII DC electrical characteristics when operating from a 3.3V supply.

Table 3-49. MII DC electrical characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * L1VDD	–	V	(1)
Input low voltage	V_{IL}	–	0.2 * L1VDD	V	(1)
Input high current (V_{IN}= $L1V_{DD}$)	I_{IH}	–	50	µA	(2)
Input low current (V_{IN}= GND)	I_{IL}	–50	–	µA	(2)
Output high voltage ($L1V_{DD}$ = min, I_{OH} = –2.0 mA)	V_{OH}	2.4	–	V	–
Output low voltage ($L1V_{DD}$ = min, I_{OL}= 2.0 mA)	V_{OL}	–	0.40	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max $L1V_{IN}$ values found in Table 3-2

2. The symbol V_{IN}, in this case, represents the $L1V_{IN}$ symbols referenced in Table for "Absolute Maximum Ratings"

This table shows the MII DC electrical characteristics when operating from a 2.5V supply.

Table 3-50. MII DC electrical characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * L1VDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * L1VDD	V	1
Input high current (V_{IN}= $L1V_{DD}$)	I_{IH}	–	50	µA	2
Input low current (V_{IN}= GND)	I_{IL}	–50	–	µA	2
Output high voltage ($L1V_{DD}$ = min, I_{OH} = –1.0 mA)	V_{OH}	2.0	–	V	–
Output low voltage ($L1V_{DD}$ = min, I_{OL}= 1.0 mA)	V_{OL}	–	0.40	V	–

3.11.5.2 MII AC timing specifications

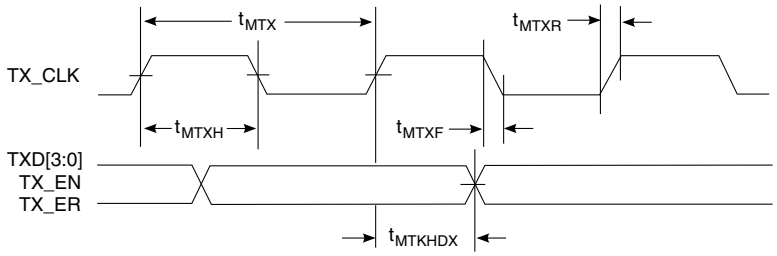
This section describes the MII transmit and receive AC timing specifications.

Table 3-51. MII transmit AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	–	400	–	ns
TX_CLK clock period 100 Mbps	t_{MTX}	–	40	–	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	–	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	–	25	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	–	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	–	4.0	ns

This figure shows the MII transmit AC timing diagram.

Figure 3-17. MII transmit AC timing diagram



This table provides the MII receive AC timing specifications.

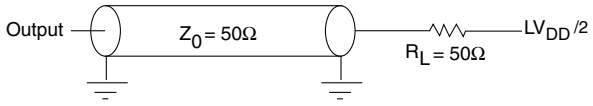
Table 3-52. MII receive AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	–	400	–	ns
RX_CLK clock period 100 Mbps	t_{MRX}	–	40	–	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	–	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	–	–	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	–	–	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	–	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	–	4.0	ns

Notes: 1. The frequency of RX_CLK (input) should not exceed the frequency of TX_CLK (input) by more than 300 ppm.
2. For recommended operating conditions, see Table 3-2

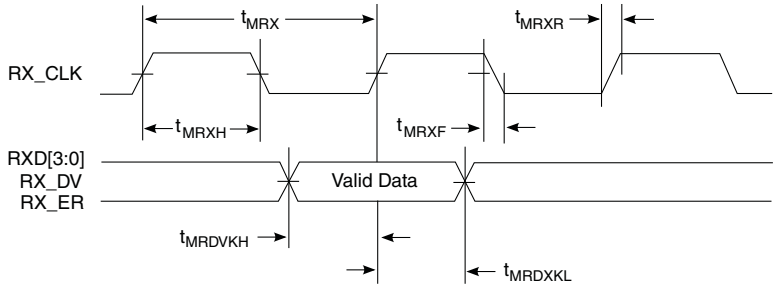
This figure provides the AC test load for the Ethernet controller.

Figure 3-18. Ethernet controller AC test load



This figure shows the MII receive AC timing diagram.

Figure 3-19. MII receive AC timing diagram



3.11.6 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 interface. The EMI1 interface timing is compatible with IEEE Std 802.3ô clause 22.

3.11.6.1 Ethernet management interface 1 DC electrical characteristics

The DC electrical characteristics for EMI1_MDIO and EMI1_MDC are provided in this section. The pins are available on LV_{DD} and $L1V_{DD}$. Refer to Table 3-2 for operating voltages.

Table 3-53. Ethernet management interface 1 DC electrical characteristics ($L1V_{DD}$ = 3.3V)(3)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * L1VDD	–	V	(1)
Input low voltage	V_{IL}	–	0.2 * L1VDD	V	(1)
Input current (LV_{IN} = 0V or LV_{IN}= LV_{DD})	I_{IN}	–	±50	µA	(2)
Output high voltage ($L1V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage ($L1V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max $L1V_{IN}$ values found in Table 3-2.
2. The symbol LV_{IN}, in this case, represents the $L1V_{IN}$ symbol referenced in Recommended operating conditions
3. For recommended operating conditions, see Table 3-2

Table 3-54. Ethernet management interface 1 DC electrical characteristics (LV_{DD}= 2.5V)3, 4

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * LVDD	V	1, 4
Input high current (V_{IN} = LV_{DD})	I_{IH}	–	50	µA	2, 4
Input low current (V_{IN} = GND)	I_{IL}	–50	–	µA	–
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.40	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN}/$L1V_{IN}$ values found in Table 3-2.
2. The symbol V_{IN}, in this case, represents the LV_{IN}/$L1V_{IN}$ symbols referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. The symbol LV_{DD}, in this case, represents the LV_{DD}/$L1V_{DD}$ symbols referenced in Recommended operating conditions.

Table 3-55. Ethernet management interface 1 DC electrical characteristics(1.8V)3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * LVDD	V	1, 4
Input current (LV_{IN} = 0V or LV_{IN} = LV_{DD})	I_{IN}	–	±50	µA	2, 4
Output high voltage (LV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	4
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	4

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN}/$L1V_{IN}$ respective values found in Table 3-2.
2. The symbol LV_{IN} represents the LV_{IN}/$L1V_{IN}$ symbols referenced in Recommended operating conditions.

3. For recommended operating conditions, see Table 3-2.
4. The symbol LV_{DD}, in this case, represents the LV_{DD} and $L1V_{DD}$ symbols referenced in Recommended operating conditions.

3.11.6.2 Ethernet management interface 1 AC electrical specifications

This table provides the Ethernet management interface 1 AC timing specifications.

Table 3-56. Ethernet management interface 1 AC timing specifications(5)

Parameter/Condition	Symbol(1)	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	–	–	2.5	MHz	(2)
MDC clock pulse width high	t_{MDCH}	160	–	–	ns	–
MDC to MDIO delay	t_{MDKHDX}	$(5 \times t_{enet\_clk}) - 3$	–	$(5 \times t_{enet\_clk}) + 3$	ns	(3)(4)
MDIO to MDC setup time	t_{MDDVKH}	8	–	–	ns	–
MDIO to MDC hold time	t_{MDDXKH}	0	–	–	ns	–

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.
4. t_{enet_clk} is the Ethernet clock period (Frame Manager clock period × 2).
5. For recommended operating conditions, see Table 3-2.

3.11.7 IEEE 1588 electrical specifications

3.11.7.1 IEEE 1588 DC electrical characteristics

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 3.3V supply.

Table 3-57. IEEE 1588 DC electrical characteristics(LV_{DD} = 3.3V)(3)

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	(1)
Input low voltage	V_{IL}	–	0.2 * LVDD	V	(1)
Input current (LV_{IN}= 0V or LV_{IN}= LV_{DD})	I_{IH}	–	±50	µA	(2)
Output high voltage (LV_{DD} = min, I_{OH} = –2.0 mA)	V_{OH}	2.4	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 2.0 mA)	V_{OL}	–	0.40	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5V supply.

Table 3-58. IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * LVDD	V	1
Input current (LV_{IN}= 0V or LV_{IN}= LV_{DD})	I_{IH}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.40	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8V supply.

Table 3-59. IEEE 1588 DC electrical characteristics(LV_{DD} = 1.8V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * LVDD	V	1
Input current (LV_{IN}= 0V or LV_{IN}= LV_{DD})	I_{IH}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.40	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

3.11.7.2 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

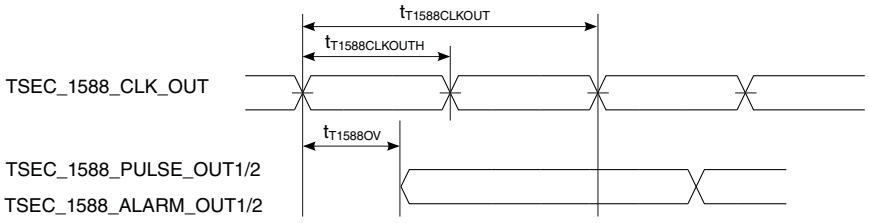
Table 3-60. IEEE 1588 AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	FM_CLK/2	–	$T_{RX\_CLK} \times 7$	ns	(1)(3)(6)
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	(2)
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	–	–	250	ps	–
Rise time TSEC_1588_CLK_IN (20%-80%)	$t_{T1588CLKINR}$	1.0	–	2.0	ns	–
Fall time TSEC_1588_CLK_IN (80%-20%)	$t_{T1588CLKINF}$	1.0	–	2.0	ns	–
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	–	–	ns	(4)
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	–
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	–	3.0	ns	–
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	–	–	ns	(3)

Notes:
1. T_{RX_CLK} is the maximum clock period of ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.
4. There are 3 input clock sources for 1588 that is, TSEC_1588_CLK_IN, RTC and MAC clock / 2. When using TSEC_1588_CLK_IN, the minimum clock period is $2 \times t_{T1588CLK}$.
5. For recommended operating conditions, see Table 3-2.
6. FM_CLK = platform clock

This figure shows the data and command output AC timing diagram.

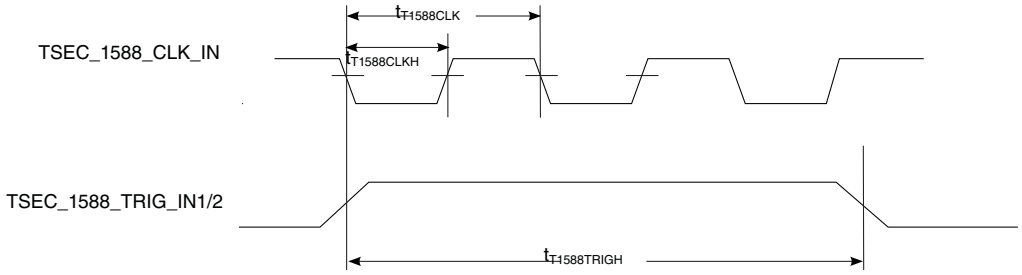
Figure 3-20. EEE 1588 output AC timing



Note: The output delay is counted starting at the rising edge if tT1588CLKOUT is non-inverting. Otherwise, it is counted starting at the falling edge.

This figure shows the data and command input AC timing diagram.

Figure 3-21. IEEE 1588 input AC timing



3.12 QUICC Engine Specifications

3.12.1 HDLC, Transparent, and Synchronous UART interfaces

This section describes the DC and AC electrical specifications for the high level data link control HDLC, transparent and synchronous UART.

3.12.1.1 HDLC, Transparent and Synchronous UART DC electrical characteristics

This table provides the DC electrical characteristics for the HDLC, Transparent and Synchronous UART protocols.

Table 3-61. HDLC, Transparent and Synchronous UART DC electrical characteristics (DVDD=3.3V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	(1)
Input low voltage	V_{IL}	–	0.2 * DVDD	V	(1)
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	(2)
Output high voltage (DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	–	0.4	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2

2. The symbol V_{IN}, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.

3. For recommended operating conditions, see Table 3-2.

This table provides the DC electrical characteristics for the HDLC, Transparent and Synchronous UART protocols.

Table 3-62. HDLC, Transparent and Synchronous UART DC electrical characteristics (DVDD=2.5V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (DV_{DD} = min, I_{OH} = 1 mA)	V_{OL}	–	0.4	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2

2. The symbol V_{IN}, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.

3. For recommended operating conditions, see Table 3-2.

3.12.1.2 *HDLC, Transparent and Synchronous UART AC timing specifications*

This table provides the input and output AC timing specifications for HDLC, and Transparent and Synchronous UART protocols.

Table 3-63. HDLC, Transparent AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-Internal clock delay	t_{HIKHOV}	0	5.5	ns	1
Outputs-External clock delay	t_{HEKHOV}	1	8.5	ns	1
Outputs-Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns	1
Outputs-External clock High Impedance	t_{HEKHOX}	1	8.2	ns	1
Inputs-Internal clock input setup time	t_{HIIVKH}	8.0	–	ns	–
Inputs-External clock input setup time	t_{HEIVKH}	4	–	ns	–
Inputs-Internal clock input Hold time	t_{HIIXKH}	0	–	ns	–
Inputs-External clock input hold time	t_{HEIXKH}	1	–	ns	–

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 3-2.
3. The Maximum frequency of operation is 50MHz

This table provides the input and output AC timing specifications for the synchronous UART protocols.

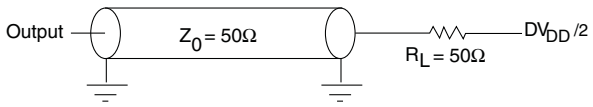
Table 3-64. Synchronous UART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-Internal clock delay	t_{HIKHOV}	0	11	ns	1
Outputs-External clock delay	t_{HEKHOV}	1	14	ns	1
Outputs-Internal clock High Impedance	t_{HIKHOX}	0	11	ns	1
Outputs-External clock High Impedance	t_{HEKHOX}	1	14	ns	1
Inputs-Internal clock input setup time	t_{HIIVKH}	10	–	ns	–
Inputs-External clock input setup time	t_{HEIVKH}	8	–	ns	–
Inputs-Internal clock input Hold time	t_{HIIXKH}	0	–	ns	–
Inputs-External clock input hold time	t_{HEIXKH}	1	–	ns	–

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 3-2.

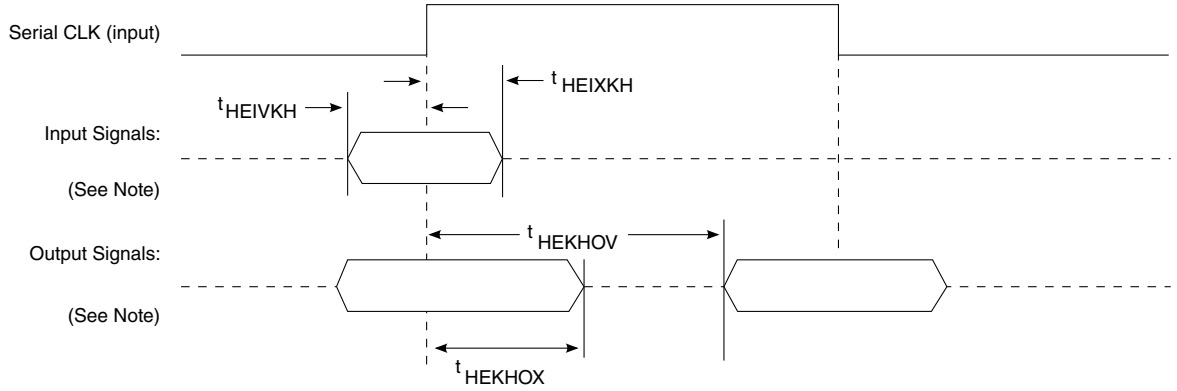
This figure provides the AC test load.

Figure 3-22. AC test load



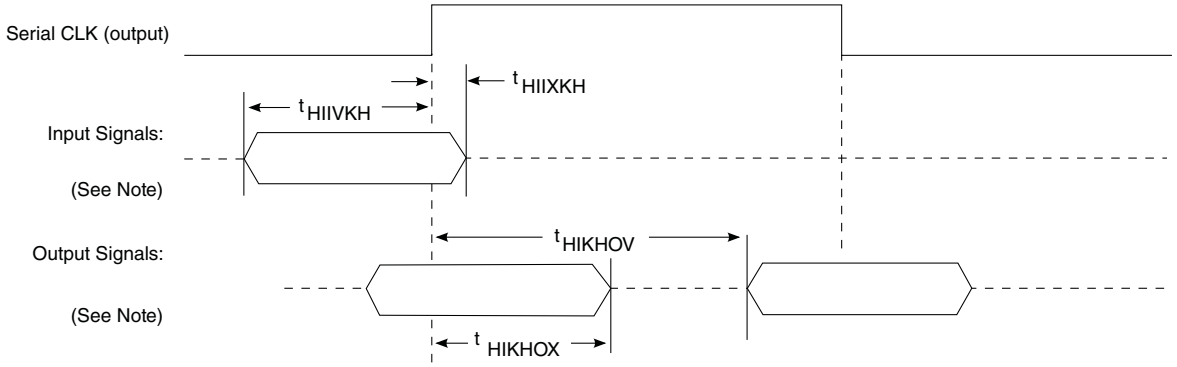
These figures represent the AC timing from Table 3-63 on page 88 and Table 3-64. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. This figure shows the timing with external clock.

Figure 3-23. AC timing (external clock) diagram



This figure shows the timing with internal clock.

Figure 3-24. AC timing (internal clock) diagram



Note: The clock edge is selectable

3.12.2 TDM/SI

This section describes the DC and AC electrical specifications for the time-division- multiplexed and serial interface (TDM/SI).

3.12.2.1 TDM/SI DC electrical characteristics

This table provides the TDM/SI DC electrical characteristics.

Table 3-65. TDM/SI DC electrical characteristics (DVDD=3.3V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2 on page 43
2. The symbol V_{IN}, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

Table 3-66. TDM/SI DC electrical characteristics (DVDD=2.5V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (DV_{DD} = min, I_{OH} = 1 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2
2. The symbol V_{IN}, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

3.12.2.2 TDM/SI AC timing specifications

This table provides the TDM/SI input and output AC timing specifications.

Table 3-67. TDM/SI AC timing specifications 1

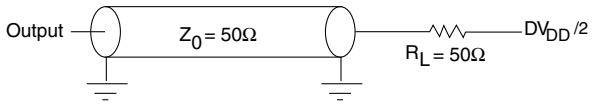
Parameter	Symbol [1]	Min	Max	Unit
TDM/SI outputs-External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs-External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs-External clock input setup time	t_{SEIVKH}	5	–	ns
TDM/SI inputs-External clock input hold time	t_{SEIXKH}	2	–	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 3-2.

NOTE
The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of DV_{DD}; fall time refers to transitions from 90% to 10% of DV_{DD}

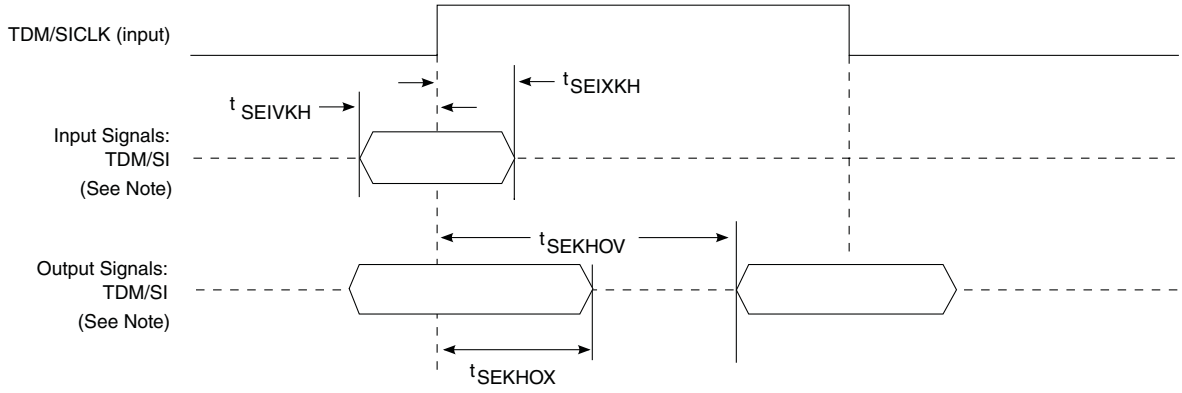
This figure provides the AC test load for the TDM/SI.

Figure 3-25. TDM/SI AC test load



This figure represents the AC timing from Table 3-65. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. This figure shows the TDM/SI timing with external clock.

Figure 3-26. TDM/SI AC timing (external clock) diagram



3.13 USB interface

This section provides the AC and DC electrical specifications for the USB interface.

3.13.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at USB_HV_{DD} = 3.3V.

Table 3-68. USB DC electrical characteristics (USB_HV_{DD} = 3.3V) [3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	–	V	1
Input low voltage	V_{IL}	–	0.8	V	1
Input current (USB_HV_{IN} = 0V or USB_HV_{IN} = USB_HV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (USB_HV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	–	V	–
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.3	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 3-2.
2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Recommended operating conditions
3. For recommended operating conditions, see Table 3-2

This table provides the DC electrical characteristics for the USBCLK at $O1V_{DD}$ = 1.8V.

Table 3-69. USBCLK DC electrical characteristics (1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	–	V	1
Input low voltage	V_{IL}	–	0.6	V	1
Input current (V_{IN} = 0V or V_{IN} = $O1V_{DD}$)	I_{IN}	–	±50	µA	2

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max $O1V_{IN}$ values found in Table 3-2.
2. The symbol V_{IN}, in this case, represents the $O1V_{IN}$ symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

3.13.2 USB AC timing specifications

This section describes the AC timing specifications for the on-chip USB PHY. See Chapter 7 in the *Universal Serial Bus Revision 2.0 Specification* for more information.

This table provides the USB clock input (USBCLK) AC timing specifications.

Table 3-70. USBCLK AC timing specifications[(1)]

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	–	$f_{USB\_CLK\_IN}$	–	24	–	MHz	–
Rise/Fall time	Measured between 10% and 90%	t_{USRF}	–	–	6	ns	[(2)]
Clock frequency tolerance	–	t_{CLK_TOL}	–0.005	0	0.005	%	–
Reference clock duty cycle	Measured at rising edge and/or failing edge at $O1V_{DD}/2$	t_{CLK_DUTY}	40	50	60	%	–
Total input jitter/time interval error	RMS value measured with a second-order, band-pass filter of 500 kHz to 4 MHz bandwidth at 10^{-12} BER	t_{CLK_PJ}	–	–	5	ps	–

Notes:
1. For recommended operating conditions, see Table 3-2
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.14 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.14.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD}= 1.8V.

Table 3-71. Integrated flash controller DC electrical characteristics (1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	–	V	1
Input low voltage	V_{IL}	–	0.6	V	1
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (OV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.32	V	–

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3-2.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

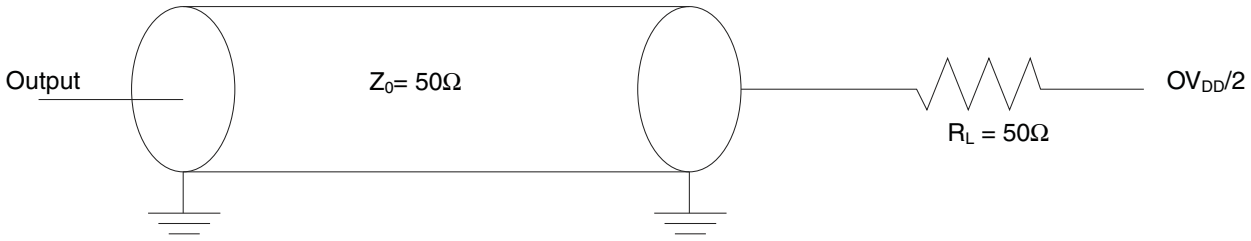
3.14.2 Integrated flash controller AC timing

This section describes the AC timing specifications for the integrated flash controller.

3.14.2.1 Test condition

This figure provides the AC test load for the integrated flash controller.

Figure 3-27. Integrated flash controller AC test load



3.14.2.2 Integrated flash controller Input AC timing specifications

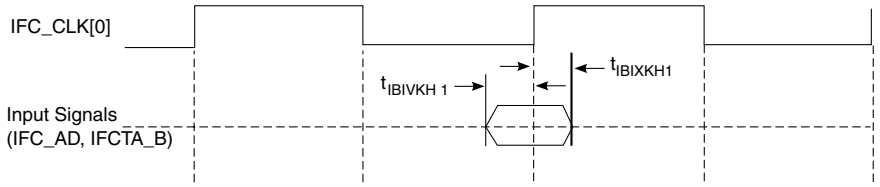
This table describes the input AC timing specifications of the IFC-GPCM and IFC- GASIC interface.

Table 3-72. Integrated Flash Controller input timing specifications for GPCM and GASIC mode (OVDD = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	–	ns	–
Input hold	$t_{IBIXKH1}$	1	–	ns	–

This figure shows the input AC timing diagram for IFC-GPCM, IFC-GASIC interface.

Figure 3-28. IFC-GPCM, IFC-GASIC input AC timings



This table describes the input timing specifications of the IFC-NOR interface.

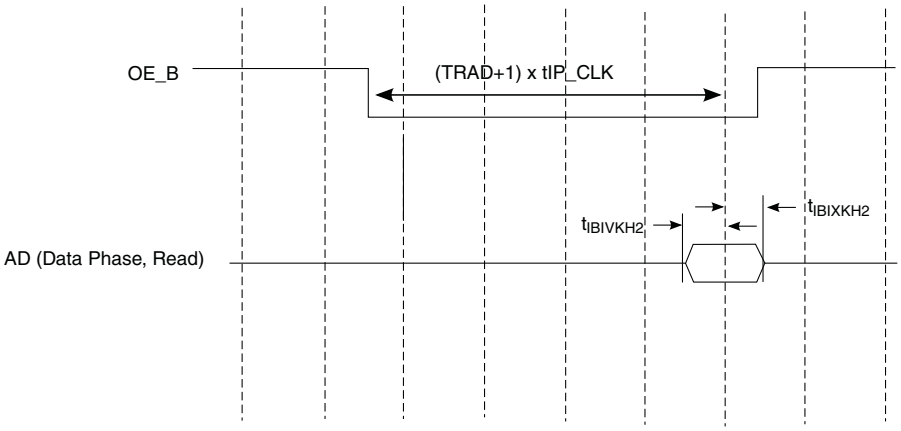
Table 3-73. Integrated Flash Controller Input timing specifications for NOR mode (OV_{DD} = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	$(2 \times t_{IP\_CLK}) + 2$	–	ns	1
Input hold	$t_{IBIXKH2}$	$^{1} \times t_{IP\_CLK}$	–	ns	1

Notes: 1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 3-2

This figure shows the AC input timing diagram for input signals of IFC-NOR interface. Here TRAD is a programmable delay parameter, refer to IFC section of QT1040 Qormino Integrated Processor Reference Manual for more information.

Figure 3-29. IFC-NOR Interface input AC timings



IP_CLK is the internal clock on which IFC is running. It is not available on interface pins.

This table describes the input timing specifications of the IFC-NAND interface.

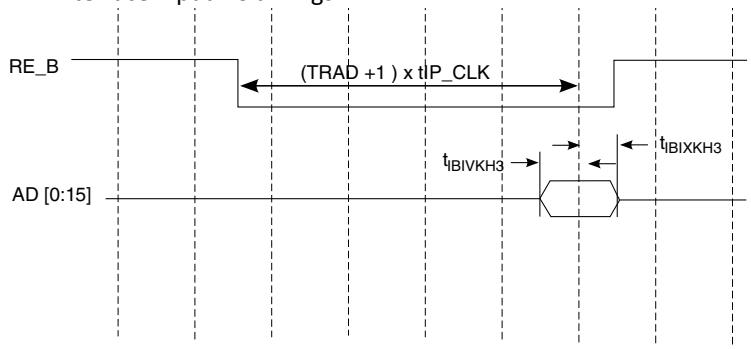
Table 3-74. Integrated Flash Controller input timing specifications for NAND mode (OV_{DD} = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	$(^{2} \times t_{IP\_CLK}) + 2$	–	ns	1
Input hold	$t_{IBIXKH3}$	$(^{1} \times t_{IP\_CLK})$	–	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	–	t_{IP_CLK}	1

Notes: 1. t_{IP_CLK} is the period of ip clock on which IFC is running.
2. For recommended operating conditions, see Table 3-2

This figure shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter, refer to IFC section of QT1040 Qormino Integrated Processor Reference Manual for more information.

Figure 3-30. IFC-NAND Interface input AC timings



t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

3.14.2.3 Integrated flash controller output AC timing specifications

This table describes the output AC timing specifications of IFC-GPCM and IFC-GASIC interface.

Table 3-75. Integrated Flash Controller IFC-GPCM and IFC-GASIC interface output timing specifications (OV_{DD} = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	–	ns	–
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	–
Output delay	$t_{IBKLOV1}$	–	1.5	ns	–
Output hold	t_{IBKLOX}	–	–2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	–

Notes: 1. Output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 3-2

This figure shows the output AC timing diagram for IFC-GPCM, IFC-GASIC interface.

Figure 3-31. IFC-GPCM, IFC-GASIC Signals

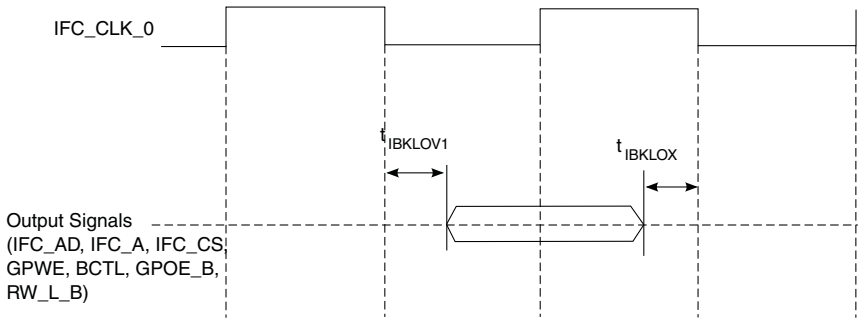


Table 3-76. Integrated Flash Controller IFC-NOR Interface output timing specifications (OV_{DD} = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	–	±1.5	ns	1

Notes: 1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3-2

This figure shows the AC timing diagram for output signals of IFC-NOR interface. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. OE_B is suppose to change TACO (a programmable delay, refer to IFC section of QT1040 Qormino Integrated Processor Reference Manual for more information) time after CS_B. Because of skew between the signals, OE_B may change anywhere within time window $t_{IBKLOV2}$ (min) and $t_{IBKLOV2}$ (max). This concept applies to other output signals of IFC-NOR interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. Here is the list of IFC-NOR output signals NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD(Address phase).

Figure 3-32. IFC-NOR Interface Output AC Timings

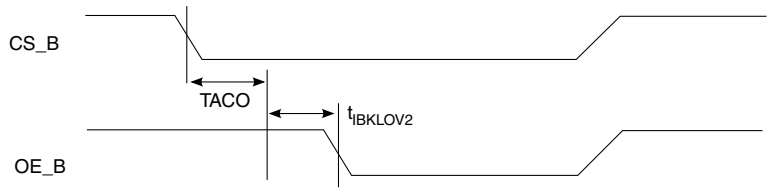


Table 3-77. Integrated Flash Controller IFC-NAND Interface output timing specifications (OV_{DD} = 1.8V)

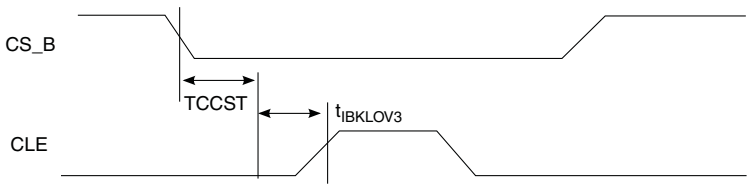
Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	–	±1.5	ns	1

Notes: 1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 3-2

This figure shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs have been illustrated here by taking timings between two signals, CS_B and CLE as an example. CLE is suppose to change TCCST (a programmable delay, refer to IFC section of QT1040 Qormino Integrated Processor Reference Manual for more information) time after CS_B. Because of skew between the signals CLE may change anywhere within time window $t_{IBKLOV3}$ (min) and $t_{IBKLOV3}$ (max). This concept applies to other output signals of IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. Here is the list of output signals NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, AD.

Figure 3-33. IFC-NAND Interface Output AC Timings



3.14.2.4 Integrated flash controller NAND Source Synchronous Interface AC timing specifications

This table describes the AC timing specifications of IFC-NAND Source Synchronous interface.

Table 3-78. Integrated Flash Controller IFC-NAND Source Synchronous Interface AC Timing Specifications (OV_{DD} = 1.8V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Command/address DQ hold time	t_{CAH}	O	2.5	–	ns	–
CLE and ALE hold time	t_{CALH}	O	2.5	–	ns	–
CLE and ALE setup time	t_{CALS}	O	2.5	–	ns	–
Command/address DQ setup time	t_{CAS}	O	2.5	–	ns	–
CE# hold time	t_{CH}	O	2.5	–	ns	–
Data DQ setup time	t_{DS}	O	1	–	ns	–
Data DQ hold time	t_{DH}	O	1	–	ns	–
Average clock cycle time	t_{CK}(avg) or t_{CK}	O	10	–	ns	(1)
Absolute clock period	t_{CK}(abs)	O	9.5	10.5	ns	–
Clock cycle high	t_{CKH}(abs)	O	0.44	0.56	t_{CK}	(2)
Clock cycle low	t_{CKL}(abs)	O	0.44	0.56	t_{CK}	–
DQS output high pulse width	t_{DQSH}	O	0.43	0.57	t_{CK}	(3)
DQS output low pulse width	t_{DQSL}	O	0.43	0.57	t_{CK}	(3)
DQS-DQ skew, DQS to last DQ valid, per access	t_{DQSQ}	I	–	1	ns	–
Data output to first DQS latching transition	t_{DQSS}	O	0.75+150(ps)	1.15	t_{CK}	
DQS cycle time	t_{DSC}	O	10	–	ns	–
DQS falling edge to CLK rising – hold time	t_{DSH}	O	0.228	–	t_{CK}	–
DQS falling edge to CLK rising – setup time	t_{DSS}	O	0.3	–	t_{CK}	–
Input data valid window	t_{DVW}	I	2.1	–	ns	–
Half-clock period	t_{HP}	O	4.4	–	ns	–
The deviation of a given t_{CK}(abs) from t_{CK}(avg)	t_{JIT} (per)	O	–0.5	0.5	ns	–
DQ-DQS hold, DQS to first DQ to go non- valid, per access	t_{QH}	I	3.1	–	ns	–

Notes:
1. t_{CK}(avg) is the average clock period over any consecutive 200 cycle window.
2. t_{CKH}(abs) and t_{CKL}(abs) include static off set and duty cycle jitter.
3. t_{DQSL} and t_{DQSH} are relative to t_{CK} when CLK is running . If CLK is stopped during data input, then t_{DQSL} and t_{DQSH} are relative to t_{DSC}.
4. For recommended operating conditions, see Table 3-2

These figures show the AC timing diagram for IFC-NAND source synchronous interface.

Figure 3-34. Command Cycle

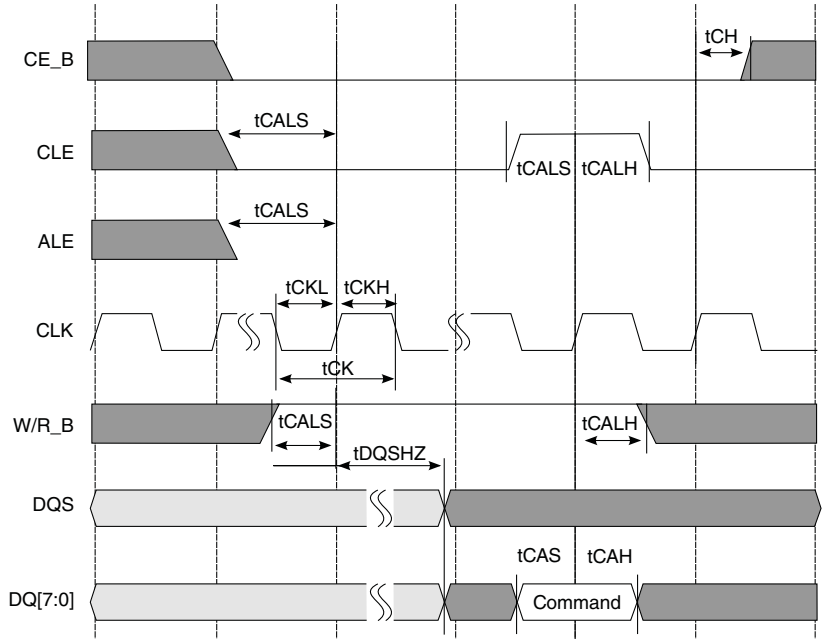


Figure 3-35. Address Cycle

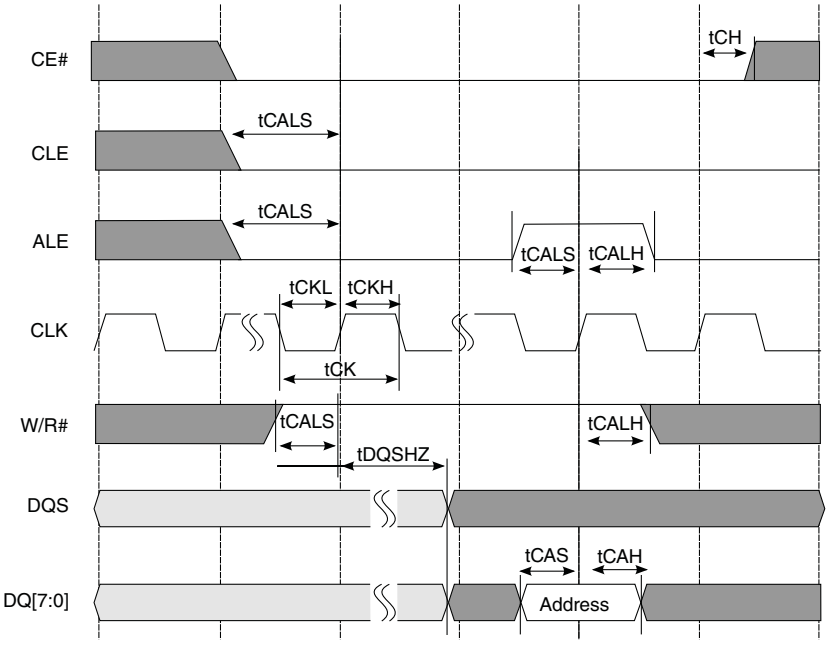


Figure 3-36. Write Cycle

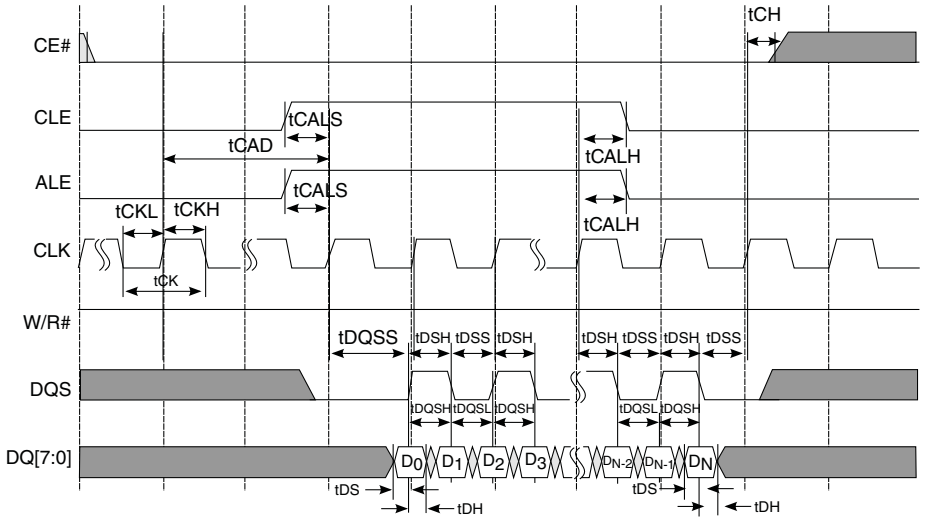
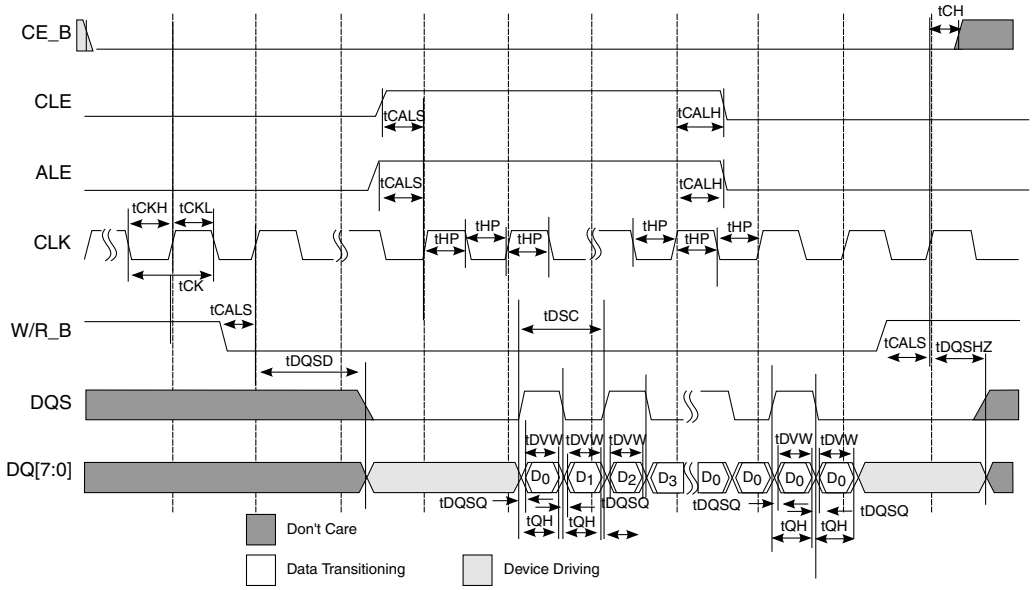


Figure 3-37. Read Cycle



3.15 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.15.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 3-79. eSDHC interface DC electrical characteristics (dual-voltage cards)[3]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	–	$0.7 \times V_{DD}$	–	V	(1)
Input low voltage	V_{IL}	–	–	$0.2 \times V_{DD}$	V	(1)
Input/Output leakage current	I_{IN}/I_{OZ}	–	–50	50	µA	–
Output high voltage	V_{OH}	I_{OH} = –100 µA at V_{DD} min	V_{DD} – 0.2V	–	V	–
Output low voltage	V_{OL}	I_{OL} = 100 µA at V_{DD} min	–	0.2	V	–
Output high voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	–	V	(2)
Output low voltage	V_{OL}	I_{OL} = 2 mA	–	0.3	V	(2)

Notes:
1. The min V_{IL} and V_{IH} values are based on the respective min and max V_{IN} values found in Table 3-2.
2. Open-drain mode is for MMC cards only.
3. For recommended operating conditions, see Table 3-2.
4. SDHC interface is powered by EV_{DD} and CV_{DD}. The V_{DD} and V_{IN} in the table above should be replaced by the respective IO power supply.

3.15.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 3-38 and Figure 3-39 (EV_{DD}/CV_{DD} = 1.8V or 3.3V).

Table 3-80. eSDHC AC timing specifications (High Speed/Full Speed)[6]

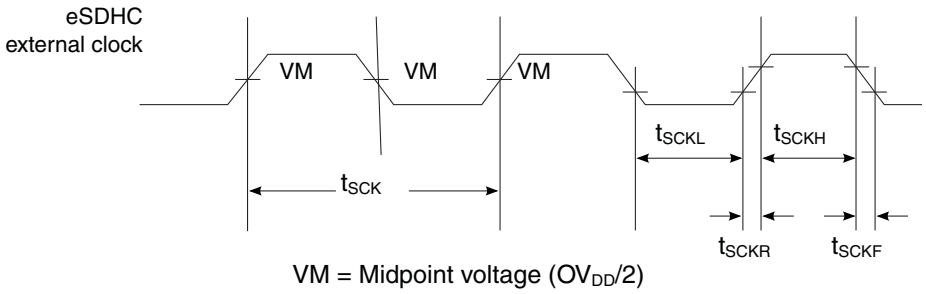
Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO (full-speed/high-speed mode)	f_{SCK}	0	25/50	MHz	2, 4
	MMC full-speed/high-speed mode			20/52		
SDHC_CLK clock low time (full-speed/high-speed mode)		t_{SCKL}	10/7	–	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)		t_{SCKH}	10/7	–	ns	4
SDHC_CLK clock rise and fall times		t_{SCKR}/ t_{SCKF}	–	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK		t_{NIIVKH}	2.5	–	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK		t_{NIIXKH}	2.5	–	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		t_{NIKHOX}	–3	–	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		t_{NIKHOV}	–	3	ns	4, 5

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and (first three letters of functional block)(reference)(state)(signal)(state) for outputs. For example, tFHSKHOV symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In full-speed mode, the clock frequency value can be 0-25 MHz for an SD/SDIO card and 0-20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50 MHz for an SD/SDIO card and 0-52 MHz for an MMC card.
3. To satisfy setup timing, one-way board-routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.
4. C_{CARD} = 10 pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ = 40 pF.
5. The parameter values apply to both full-speed and high-speed modes.
6. For recommended operating conditions, see Table 3-2

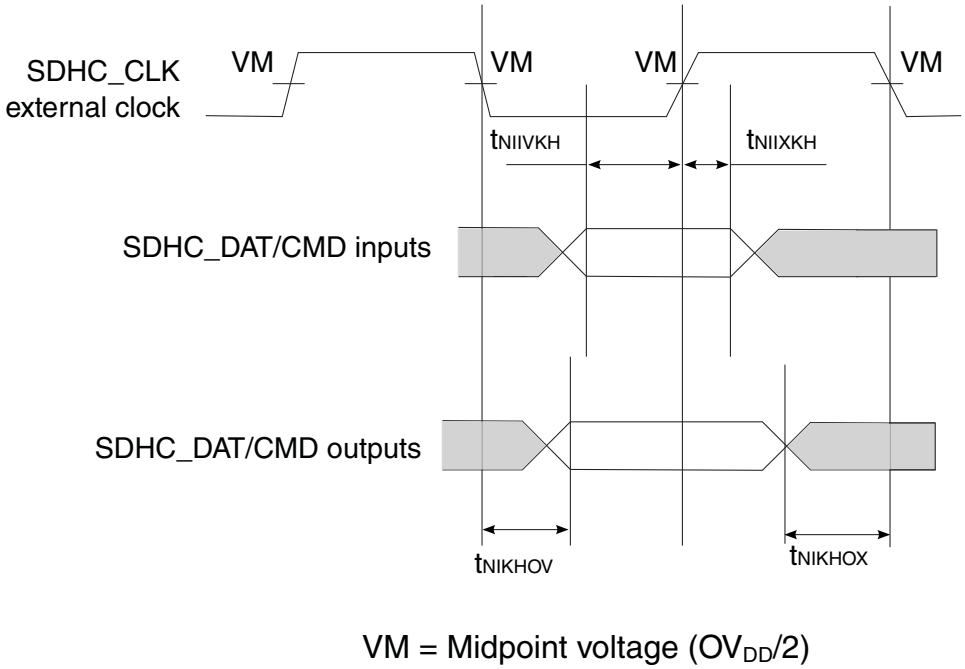
This figure provides the eSDHC clock input timing diagram.

Figure 3-38. eSDHC clock input timing diagram



This figure provides the data and command input/output timing diagram.

Figure 3-39. eSDHC data and command input/output timing diagram referenced to clock



This table provides the eSDHC AC timing specifications for SDR50 mode (EV_{DD}/CV_{DD} = 1.8V).

Table 3-81. eSDHC AC timing (SDR50)[2]

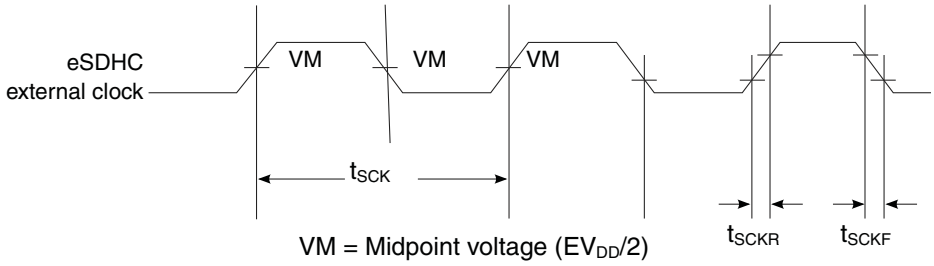
Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency:	f_{SCK}		100	MHz	
SDHC_CLK duty cycle		47	53	%	
SDHC_CLK clock rise and fall times	t_{SCKR}/ t_{SCKF}	–	2	ns	1
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	–	–0.1	0.1	ns	–
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	t_{NIIVKH}	2.1	–	ns	
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	t_{NIIXKH}	0.9	–	ns	
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	t_{NIKHOX}	2.4	–	ns	
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	t_{NIKHOV}	–	6.3	ns	

Notes: 1. C_{CARD} = 10 pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ = 30 pF.

2. For recommended operating conditions, see Table 3-2.

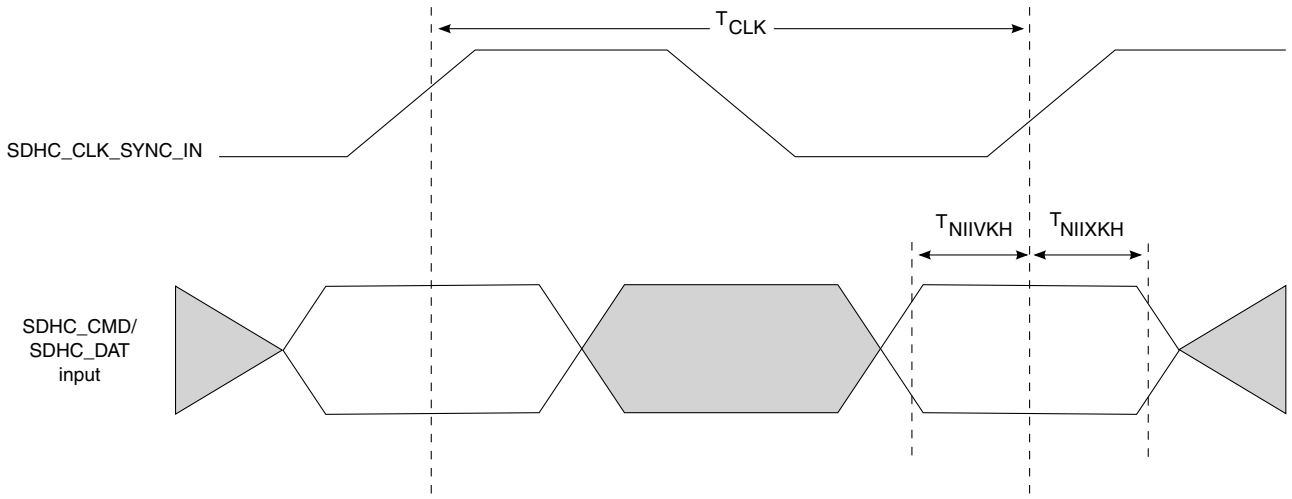
This figure provides the eSDHC clock input timing diagram for SDR50 mode.

Figure 3-40. eSDHC SDR50 mode clock input timing diagram



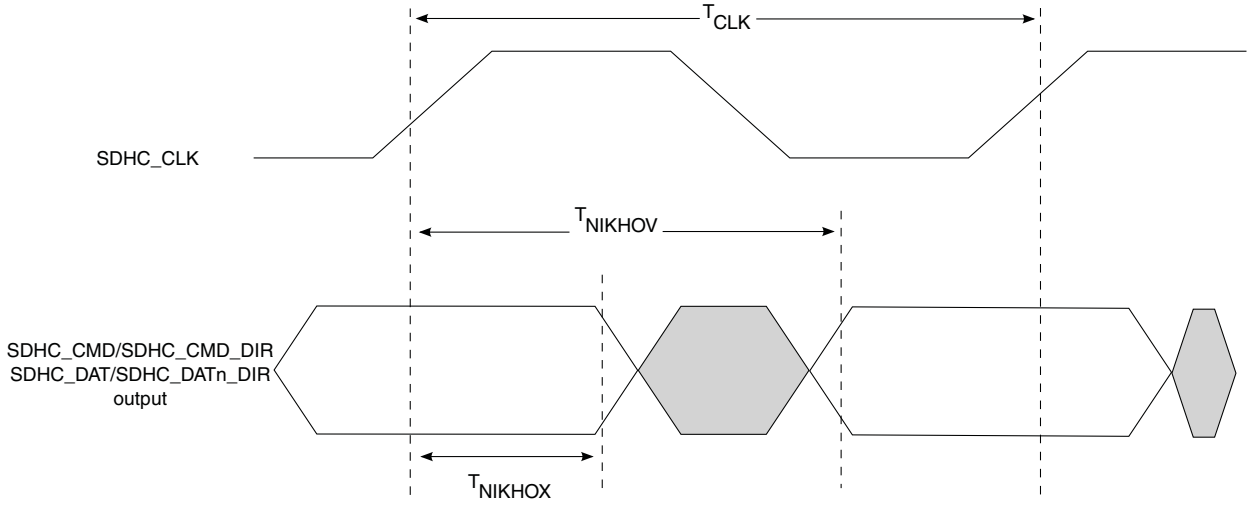
This figure shows the eSDHC input AC timing diagram for SDR50 mode.

Figure 3-41. eSDHC SDR50 mode input AC timing diagram



This figure shows the eSDHC output AC timing diagram for SDR50 mode.

Figure 3-42. eSDHC SDR50 mode output AC timing diagram



This table provides the eSDHC AC timing specifications for DDR50/eMMC DDR mode (EV_{DD}/CV_{DD} = 1.8V).

Table 3-82. eSDHC AC timing (DDR50/eMMC DDR)[3]

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	SD/SDIO DDR50 mode	f_{SCK}	–	50	MHz	–
	eMMC DDR mode			50		
SDHC_CLK duty cycle		–	47	53	%	–
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK		–	–0.1	0.1	ns	–
SDHC_CLK clock rise and fall times	SD/SDIO DDR50 mode	t_{SCKR}/ t_{SCKF}	–	4	ns	1
	eMMC DDR mode			2		2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NDIVKH}	0.5	–	ns	–
	eMMC DDR mode		0.6			
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NDIXKH}	0.98	–	ns	–
	eMMC DDR mode		0.98			
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	t_{NDKHOX}	2.2	–	ns	–
	eMMC DDR mode		3.9			
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	t_{NDKHOV}	–	5.7	ns	–
	eMMC DDR mode			6.3		
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NIIVKH}	3.3	–	ns	–
	eMMC DDR mode		2.7			

Table 3-82. eSDHC AC timing (DDR50/eMMC DDR)[3] (Continued)

Parameter		Symbol	Min	Max	Units	Notes
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NIIXKH}	0.4	–	ns	–
	eMMC DDR mode		0.4			
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	t_{NIKHOX}	2.2	–	ns	–
	eMMC DDR mode		4.4			
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	t_{NIKHOV}	–	12.2	ns	–
	eMMC DDR mode			14.6		

Notes: 1. C_{CARD} = 10 pF, (1 card).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ = 20 pF for MMC. 40pF for SD.
3. For recommended operating conditions, see Table 3-2.

This table provides the eSDHC AC timing specifications for eMMC DDR mode (EV_{DD}/CV_{DD} = 3.3V).

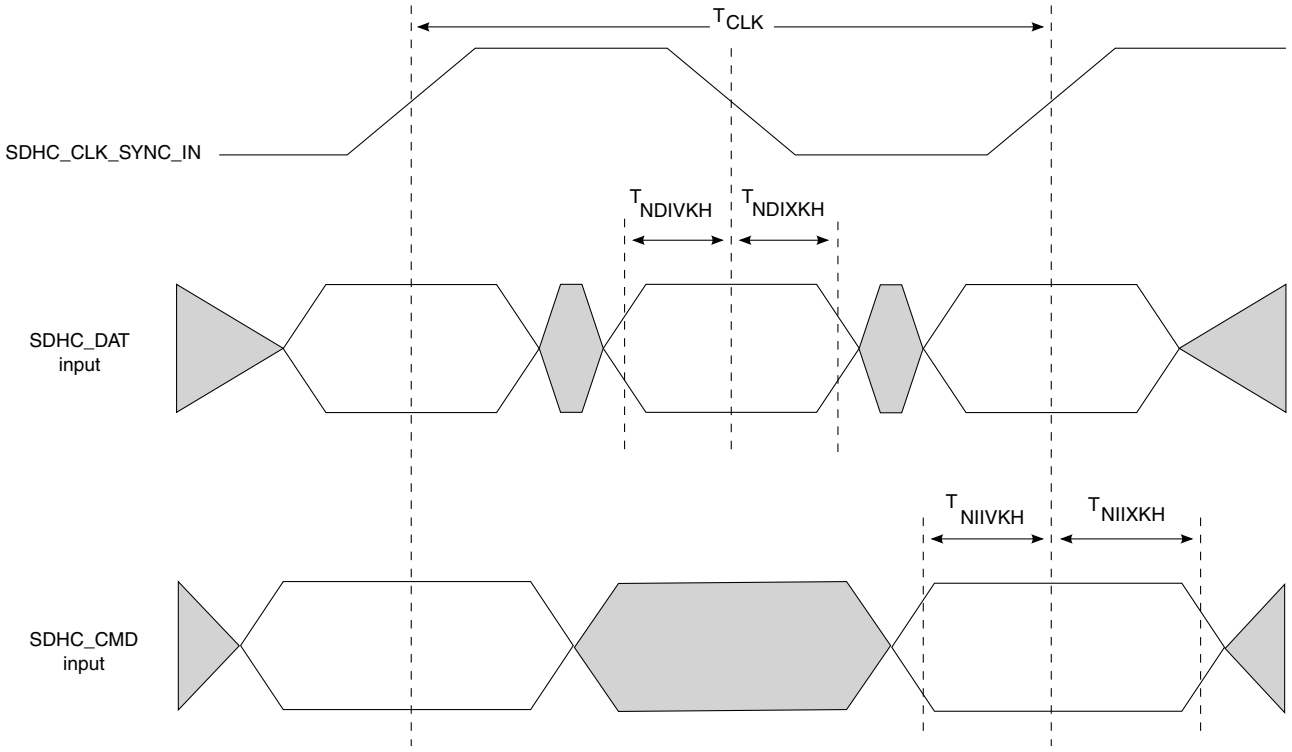
Table 3-83. eSDHC AC timing (eMMC DDR)[3]

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	eMMC DDR mode	f_{SCK}	–	49	MHz	–
SDHC_CLK duty cycle		–	47	53	%	–
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK		–	–0.1	0.1	ns	–
SDHC_CLK clock rise and fall times	eMMC DDR mode	t_{SCKR}/ t_{SCKF}	–	2	ns	2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	eMMC DDR mode	t_{NDIVKH}	1.33	–	ns	–
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	eMMC DDR mode	t_{NDIXKH}	1.32	–	ns	4
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	eMMC DDR mode	t_{NDKHOX}	3.9	–	ns	–
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	eMMC DDR mode	t_{NDKHOV}	–	6.3	ns	–
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN	eMMC DDR mode	t_{NIIVKH}	2.7	–	ns	–
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN	eMMC DDR mode	t_{NIIXKH}	0.4	–	ns	–
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	eMMC DDR mode	t_{NIKHOX}	4.4	–	ns	–
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	eMMC DDR mode	t_{NIKHOV}	–	14.6	ns	–

Notes: 1. C_{CARD} = 10 pF, (1 card).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ = 20 pF for MMC. 40pF for SD.
3. For recommended operating conditions, see Table 3-2.
4. Refer eSDHC A-008936

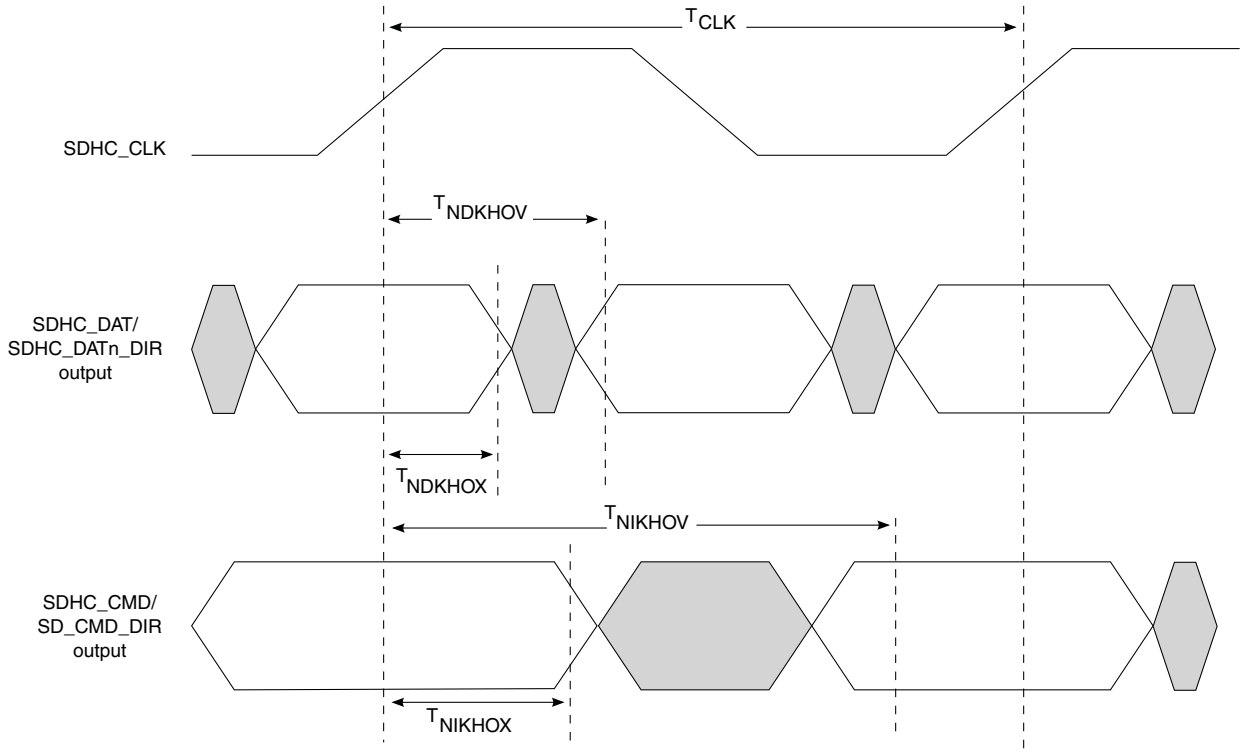
This figure shows the eSDHC DDR50/eMMC DDR mode input AC timing diagram.

Figure 3-43. eSDHC DDR50/DDR mode input AC timing diagram



This figure shows the DDR50/eMMC DDR mode output AC timing diagram.

Figure 3-44. eSDHC DDR50/DDR mode output AC timing diagram



This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode as defined in Figure 3-45 (EV_{DD}/CV_{DD} = 1.8V).

Table 3-84. eSDHC AC timing (SDR104/eMMC HS200)

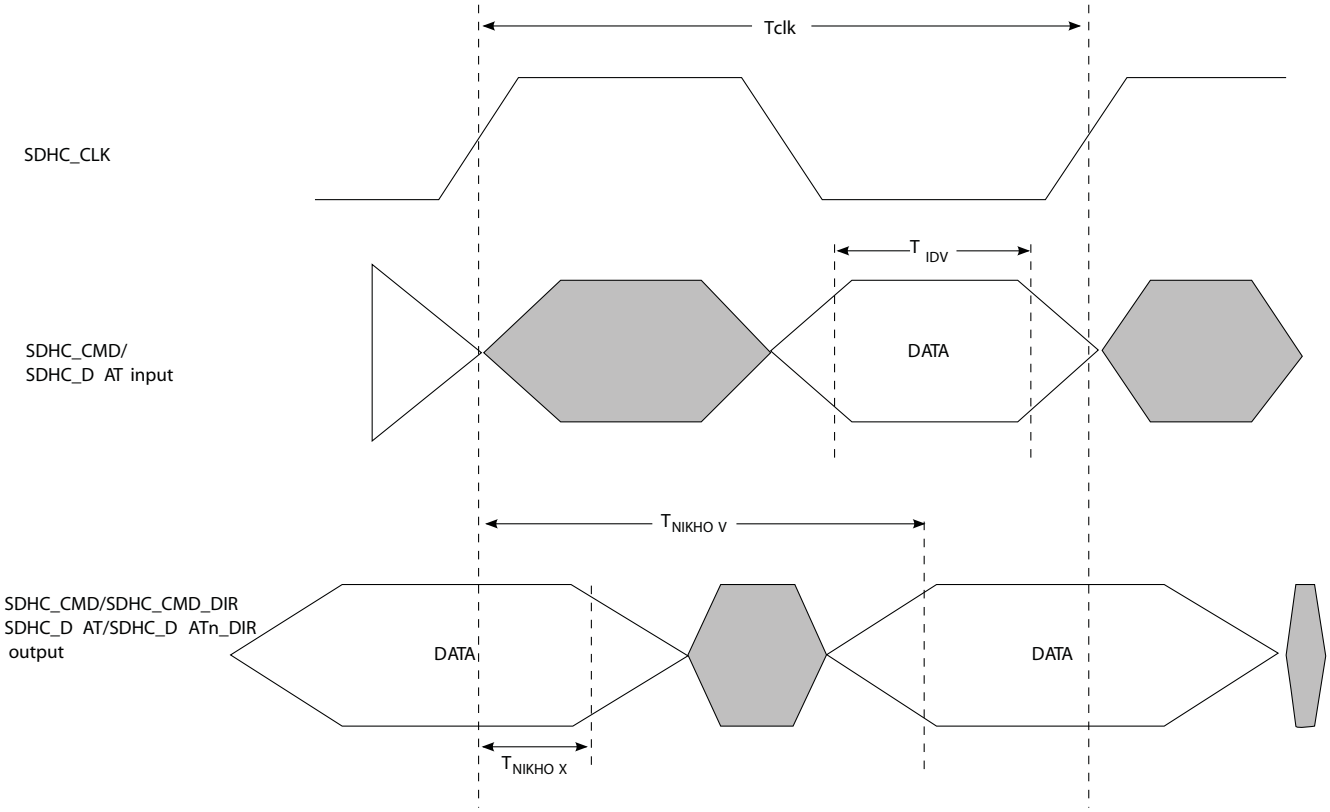
Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SCK}	–	165	MHz	–
	eMMC HS200 mode			175		
SDHC_CLK duty cycle		–	47	53	%	–
SDHC_CLK clock rise and fall times		t_{SCKR}/t_{SCKF}	–	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	t_{NIKHOX}	1.58	–	ns	–
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104	t_{NIKHOV}	–	4.15	ns	–
	eMMC HS200 mode			3.9		
Input data window (UI)	SD/SDIO SDR104 mode	t_{IDV}	0.5	–	Unit interval	–
	eMMC HS200 mode		0.475			

Notes: 1. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ = 10 pF.

2. For recommended operating conditions, see Table 3-2.

This figure provides the SDR104/HS200 mode timing diagram.

Figure 3-45. SDR104/eMMC HS200 mode timing diagram



3.16 Multicore programmable interrupt controller (MPIC)

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

3.16.1 MPIC DC specifications

These tables provides the DC electrical characteristics for the MPIC interface. IRQ's pins are on L1VDD, O1VDD, DVDD and CVDD power supplies.

Table 3-85. MPIC DC electrical characteristics ($O1V_{DD}$ = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	–	V	1
Input low voltage	V_{IL}	–	0.6	V	1
Input current ($O1V_{IN}$ = 0V or $O1V_{IN}$ = $O1V_{DD}$)	I_{IN}	–	±50	µA	2
Output high voltage ($O1V_{DD}$ = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage ($O1V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol $O1V_{IN}$, in this case, represents the $O1V_{IN}$ symbol referenced in Table 3-2.
3. For recommended operating conditions, see Table 3-2.

Table 3-86. MPIC DC electrical characteristics (DV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1, 4
Input current (DV_{IN} = 0V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol DV_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 3-2.
3. For recommended operating conditions, see Table 3-2.
4. DVDD should be replaced by the respective IO power supply i.e. L1VDD, DVDD or CVDD.

Table 3-87. MPIC DC electrical characteristics (DV_{DD} = 2.5V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1, 4
Input current (DV_{IN} = 0V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol DV_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 3-2.
3. For recommended operating conditions, see Table 3-2.
4. DVDD should be replaced by the respective IO power supply i.e. L1VDD, DVDD or CVDD.

Table 3-88. MPIC DC electrical characteristics (DV_{DD} = 3.3V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1, 4
Input current (DV_{IN} = 0V or DV_{IN} = DV_{DD})	I_{IN}	–	±40	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3-2.
2. The symbol DV_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 3-2.
3. For recommended operating conditions, see Table 3-2.
4. DVDD should be replaced by the respective IO power supply i.e. L1VDD, DVDD or CVDD.

3.16.2 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

Table 3-89. MPIC Input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
MPIC inputs-minimum pulse width	t_{PIWID}	3	–	SYSCLKs	1, 3

Note: 1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

3.17 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.17.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 3-90. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	–	V	1
Input low voltage	V_{IL}	–	0.6	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (OV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3-2.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 3-2.
3. For recommended operating conditions, see Table 3-2.

3.17.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 3-46 through Figure 3-49.

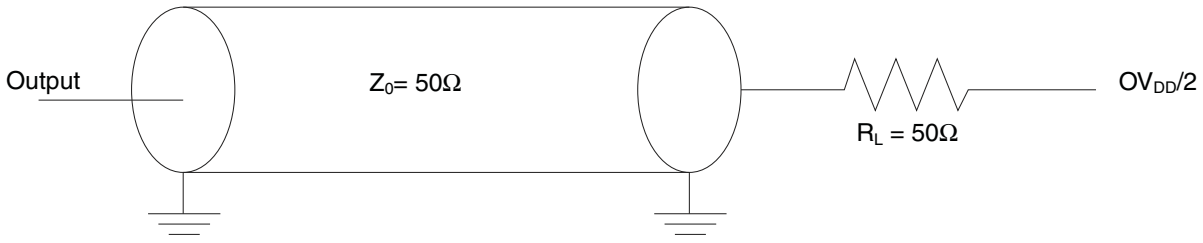
Table 3-91. JTAG AC timing specifications[4]

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	25	MHz	–
JTAG external clock cycle time	t_{JTG}	40	–	ns	–
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	–	ns	–
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	–
TRST_B assert time	t_{TRST}	25	–	ns	2
Input setup times	t_{JTDVKH}	7.5	–	ns	–
Input hold times	t_{JTDXKH}	10	–	ns	–
Output valid times	t_{JTKLDV}			ns	3
Boundary–scan data		–	15		
TDO		–	10		
Output hold times	t_{JTKLDX}	0	–	ns	3

Notes:
1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. For recommended operating conditions, see Table 3-2.

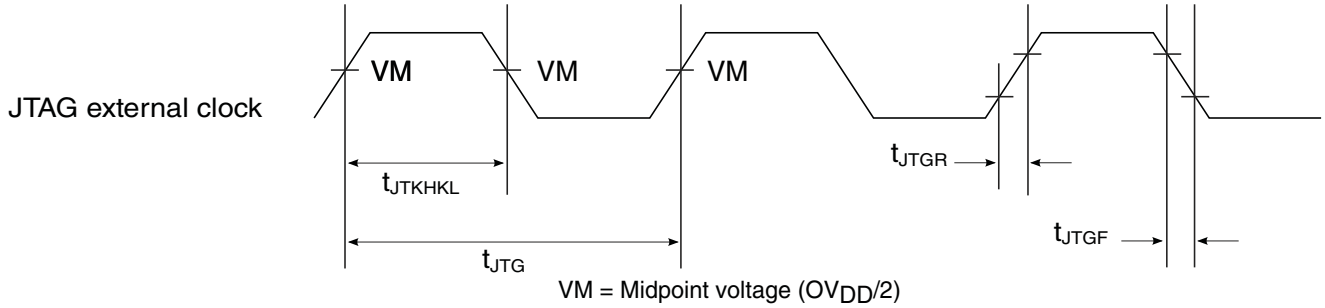
This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

Figure 3-46. AC test load for the JTAG interface



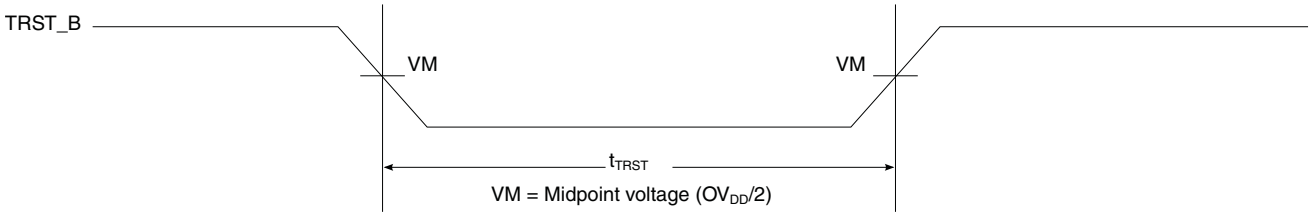
This figure provides the JTAG clock input timing diagram.

Figure 3-47. JTAG clock input timing diagram



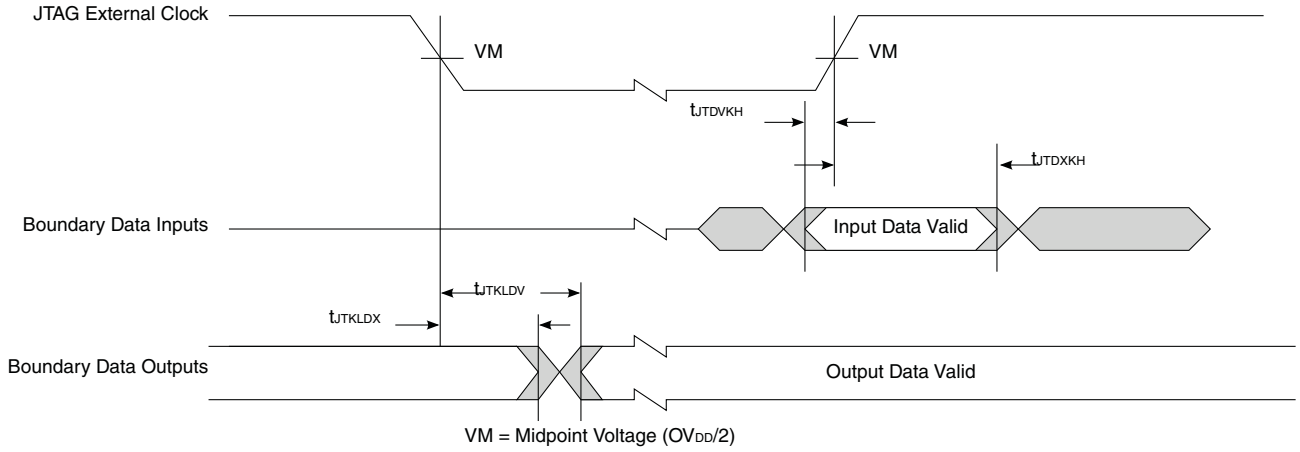
This figure provides the TRST_B timing diagram.

Figure 3-48. TRST_B timing diagram



This figure provides the boundary-scan timing diagram.

Figure 3-49. Boundary-scan timing diagram



3.18 I2C interface

This section describes the DC and AC electrical characteristics for the I^2C interface.

3.18.1 I2C DC electrical characteristics

This table provides the DC electrical characteristics for the I^2C interfaces operating at 3.3V.

Table 3-92. I^2C DC electrical characteristics (DV_{DD} = 3.3V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Output low voltage (I_{OL} = 3.0 mA)	V_{OL}	–	0.4	V	–
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × DV_{DD} and 0.9 × DV_{DD} (max)	I_i	–50	50	µA	4
Capacitance for each I/O pin	C_i	–	10	pF	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
4. For recommended operating conditions, see Table 3-2.

This table provides the DC electrical characteristics for the I^2C interfaces operating at 2.5V.

Table 3-93. I^2C DC electrical characteristics (DV_{DD} = 2.5V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.4	V	–
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × DV_{DD} and 0.9 × DV_{DD} (max)	I_i	–50	50	µA	4
Capacitance for each I/O pin	C_i	–	10	pF	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
4. For recommended operating conditions, see Table 3-2.

This table provides the DC electrical characteristics for the I²C interfaces operating at 1.8V.

Table 3-94. I²C DC electrical characteristics (DV_{DD} = 1.8V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.36	V	–
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × DV_{DD} and 0.9 × DV_{DD}(max)	I_i	–50	50	µA	4
Capacitance for each I/O pin	C_i	–	10	pF	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
4. For recommended operating conditions, see Table 3-2.

3.18.2 I²C AC timing specifications

This table provides the AC timing parameters for the I²C interfaces.

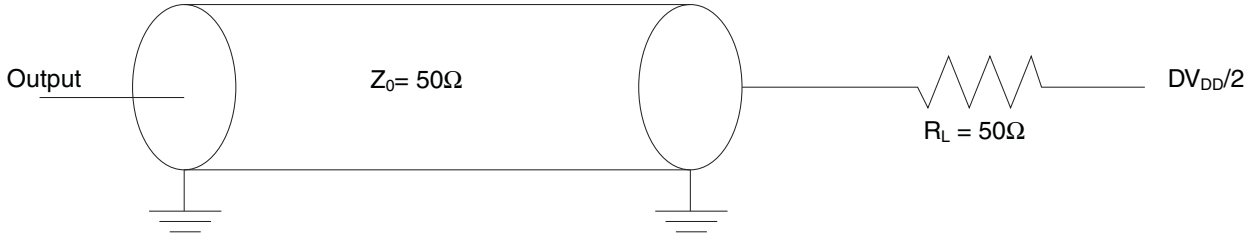
Table 3-95. I²C AC timing specifications[5]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	–	µs	–
High period of the SCL clock	t_{I2CH}	0.6	–	µs	–
Setup time for a repeated START condition	t_{I2SVKH}	0.6	–	µs	–
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	–	µs	–
Data setup time	t_{I2DVKH}	100	–	ns	–
Data input hold time:	t_{I2DXKL}			µs	3
CBUS compatible masters I²C bus devices		– 0	– –		
Data output delay time	t_{I2OVKL}	–	0.9	µs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	–	µs	–
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	–	µs	–
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	–	V	–
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	–	V	–
Capacitive load for each bus line	Cb	–	400	pF	–

Notes:
1. The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, tI2DVKH symbolizes I2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).
3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).
4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
5. For recommended operating conditions, see Table 3-2.

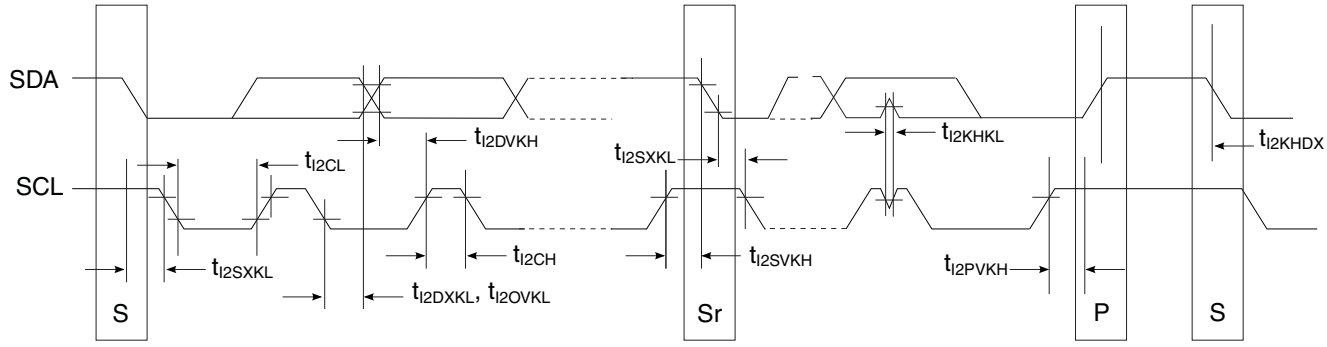
This figure provides the AC test load for the I²C.

Figure 3-50. I²C AC test load



This figure shows the AC timing diagram for the I²C bus.

Figure 3-51. I²C Bus AC timing diagram



3.19 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface. GPIO pins are on OVDD, O1VDD, DVDD, CVDD, EVDD, L1VDD and LVDD power supplies.

3.19.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at 3.3V. GPIO pins on DVDD, CVDD, EVDD, L1VDD and LVDD power supplies.

Table 3-96. GPIO DC electrical characteristics (3.3V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1, 4
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2
2. The symbol V_{IN}, in this case, represents the DV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. DVDD should be replaced by the respective IO power supply i.e. L1VDD, LVDD, EVDD or CVDD.

This table provides the DC electrical characteristics for GPIO pins operating at 2.5V. GPIO pins on DVDD, CVDD, EVDD, L1VDD and LVDD power supplies.

Table 3-97. GPIO DC electrical characteristics (2.5V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1, 4
Input current (V_{IN} = 0V or V_{IN}= DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. DVDD should be replaced by the respective IO power supply i.e. L1VDD, LVDD, EVDD or CVDD.

This table provides the DC electrical characteristics for GPIO pins operating at 1.8V. GPIO pins on DVDD, CVDD, EVDD, L1VDD and LVDD power supplies.

Table 3-98. GPIO DC electrical characteristics (1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1, 4
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1, 4
Input current (V_{IN} = 0V or V_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.
4. DVDD should be replaced by the respective IO power supply i.e. L1VDD, LVDD, EVDD or CVDD.

This table provides the DC electrical characteristics for GPIO pins operating at $O1V_{DD}/OV_{DD}$ = 1.8V.

Table 3-99. GPIO DC electrical characteristics (OVDD/O1VDD = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	–	V	1
Input low voltage	V_{IL}	–	0.6	V	1
Input current (V_{IN} = 0V or V_{IN} = OV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage ($OV_{DD}/O1V_{DD}$ = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage ($OV_{DD}/O1V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3-2.
2. The symbol V_{IN}, in this case, represents the $OV_{IN}/O1V_{IN}$ symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3-2.

3.19.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

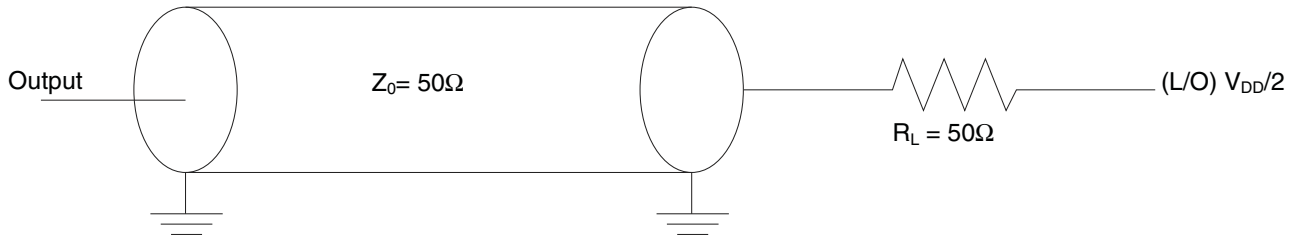
Table 3-100. GPIO input AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
GPIO inputs–minimum pulse width	t_{PIWID}	20	ns	1, 3

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 3-2.

This figure provides the AC test load for the GPIO.

Figure 3-52. GPIO AC test load



3.20 Display interface unit

This section describes the DIU DC and AC electrical characteristics.

3.20.1 DIU DC electrical characteristics

This table provides the DIU DC electrical characteristics.

Table 3-101. DIU DC electrical characteristics (3.3V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Note: 1. For recommended operating conditions, see Table 3-2.

3.20.2 DIU AC timing specifications

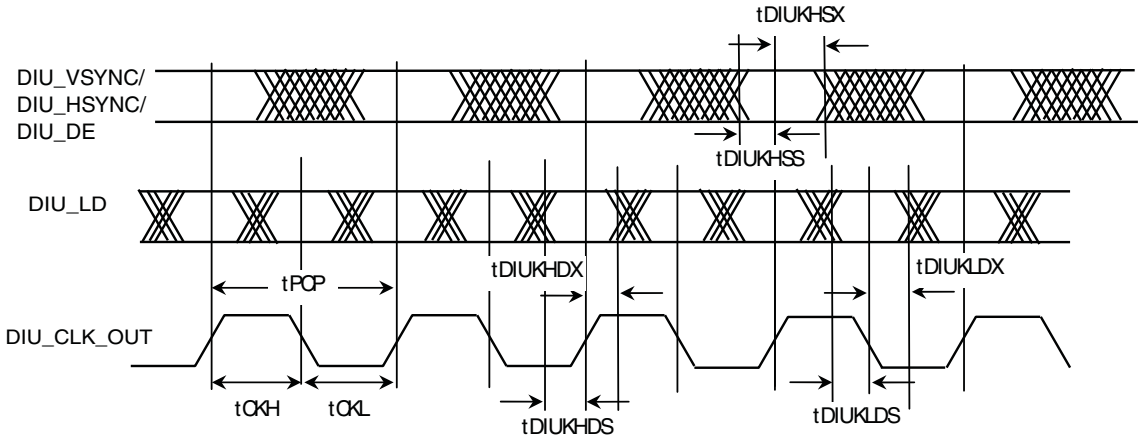
The table provides the output AC timing specifications for DIU interface.

Table 3-102. DIU interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Display pixel clock period	t_{pcp}	6.67	–	–	ns
Display pixel clock high time	t_{CKH}	0.45 × t_{PCP}	0.5 × t_{PCP}	0.55 × t_{PCP}	ns
LCD interface pixel clock low time	t_{CKL}	0.45 × t_{PCP}	0.5 × t_{PCP}	0.55 × t_{PCP}	ns
Pixel data output setup with respect to pixel clock	$t_{DIUKHDS}$ $t_{DIUKLDS}$	1.2	–	–	ns
Pixel data output hold with respect to pixel clock	$t_{DIUKHDX}$ $t_{DIUKLDX}$	1.2	–	–	ns
VSYNC/ HSYNC/ DE output setup respect to pixel clock	$t_{DIUKHSS}$	1.2	–	–	ns
VSYNC/ HSYNC/ DE output hold respect to pixel clock	$t_{DIUKHSX}$	3.8	–	–	ns

Note: 1. Display pixel clock frequency must be less than or equal to 1/4 of the platform clock.

Figure 3-53. DIU interface AC timing diagram



3.21 TDM interface

This section describes the DC and AC electrical specifications for the TDM interface.

3.21.1 TDM DC Timing Specifications

This table provides the DC electrical characteristics for the TDM interface.

Table 3-103. TDM DC Electrical Characteristics(DV_{DD} = 3.3V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * DVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 * DVDD	V	1
Input current (DV_{IN} = 0V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3-2
2. Note that the symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions
3. For recommended operating conditions, see Table 3-2

3.21.2 TDM AC Timing Specifications

This table provides the input and output AC timing specifications for the TDM interface.

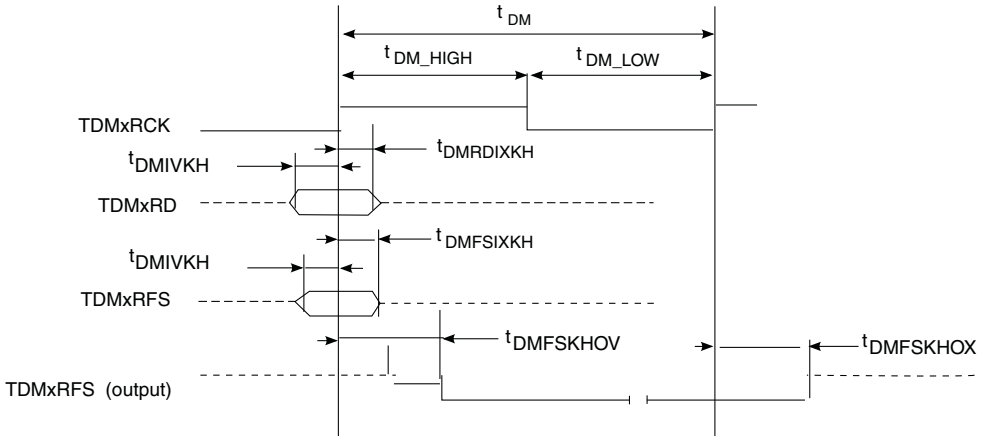
Table 3-104. TDM AC Timing Specifications for 50 MHz[1]

Characteristic	Symbol	Min	Max	Unit	Notes
TDM_RXCLK/TDM_TXCLK	t_{DM}	20.0	–	ns	–
TDM_RXCLK/TDM_TXCLK high pulse width	t_{DM_HIGH}	8.0	–	ns	–
TDM_RXCLK/TDM_TXCLK low pulse width	t_{DM_LOW}	8.0	–	ns	–
TDM all input setup time	t_{DMIVKH}	3.0	–	ns	2
TDM_RXD hold time	$t_{DMRDIXKH}$	3.5	–	ns	–
TDM_TFS/TDM_RFS input hold time	$t_{DMFSIXKH}$	2.0	–	ns	2
TDM_TXCLK high to TDM_TXD output active	t_{DM_OUTAC}	4.0	–	ns	2, 3
TDM_TXCLK high to TDM_TXD output valid	$t_{DMTKHOV}$	–	14.0	ns	2, 3
TDM_TXD hold time	$t_{DMTKHOX}$	2.0	–	ns	–
TDM_TXCLK high to TDM_TXD output high impedance	t_{DM_OUTHI}	–	10.0	ns	–
TDM_TFS/TDM_RFS output valid	$t_{DMFSKHOV}$	–	13.5	ns	2
TDM_TFS/TDM_RFS output hold time	$t_{DMFSKHOX}$	2.5	–	ns	2

Notes:
1. All values are based on a maximum TDM interface frequency of 50 MHz.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference) (state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. T_{DMxTCK} and T_{DMxRCK} are shown using the rising edge.
4. Output values are based on 30 pF capacitive load.

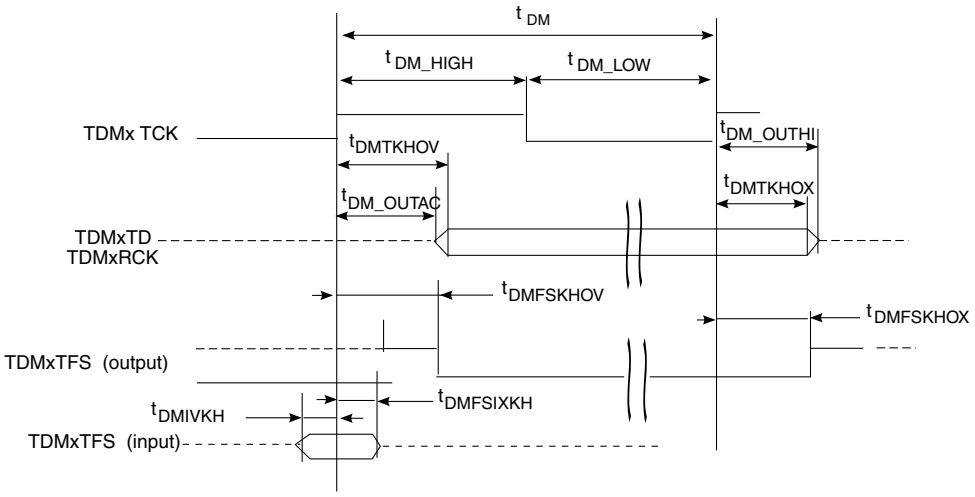
This figure shows the TDM receive signal timing.

Figure 3-54. TDM Receive Signals



This figure shows the TDM transmit signal timing.

Figure 3-55. TDM Transmit Signals



3.22 High–speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SATA, SGMII and QSGMII data transfers.

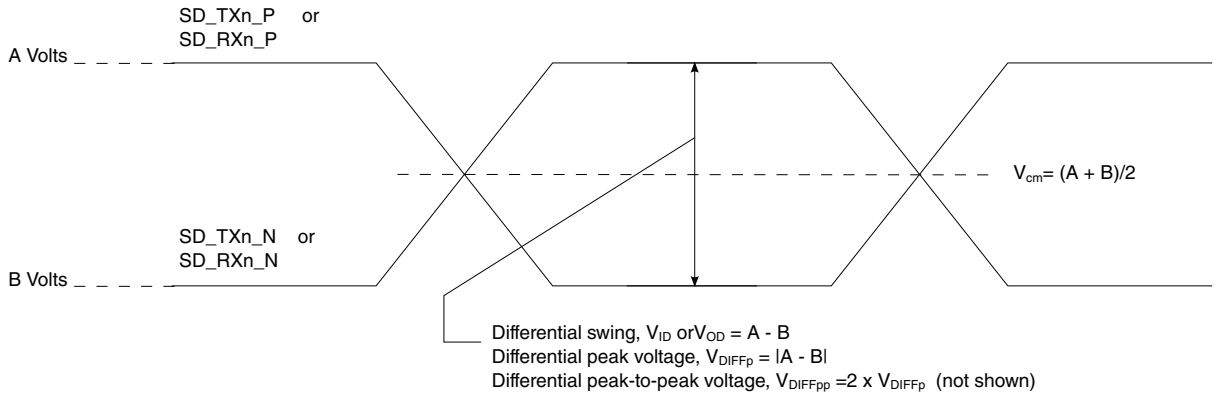
This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

3.22.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

Figure 3-56. Differential voltage definitions for transmitter or receiver



Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn\_P}$- $V_{SD\_TXn\_N.}$ The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn\_P}$- $V_{SD\_RXn\_N.}$ The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX- DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 3-61 as an example for differential waveform.

Common Mode Voltage, Vcm

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{SD\_TXn\_B})$ ˜ 2 = (A + B) ˜ 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25V and outputs, TD and TD_B. If these outputs have a swing from 2.0V to 2.5V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.22.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbaud), QSGMII (5 Gbps only)
- PEX1/2/3/4 (2.5 and 5Gbps)
- Aurora (2.5 and 5 Gbps)
- SATA1/2 (1.5 and 3.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.22.2.1 SerDes spread-spectrum clock source recommendations

SDn_REF_CLKn_P/SDn_REF_CLKn_N are designed to work with spread-spectrum clock for PCI Express protocol only with the spreading specification defined in Table 3-104. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.
For SATA protocol, the SerDes transmitter does not support spread-spectrum clocking. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread- spectrum clocking.

The spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum supported protocols. For example, if the spread- spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SATA/SGMII/QSGMII due to the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

Table 3-105. SerDes spread-spectrum clock source recommendations 1

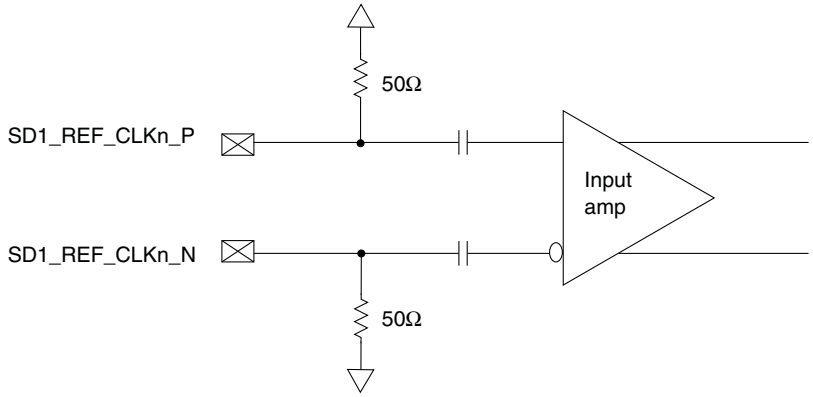
Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	–
Frequency spread	+0	–0.5	%	2

Notes: 1. At recommended operating conditions. See Table 3-2.
2. Only down-spreading is allowed.

3.22.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

Figure 3-57. Receiver of SerDes reference clocks



The characteristics of the clock signals are as follows:

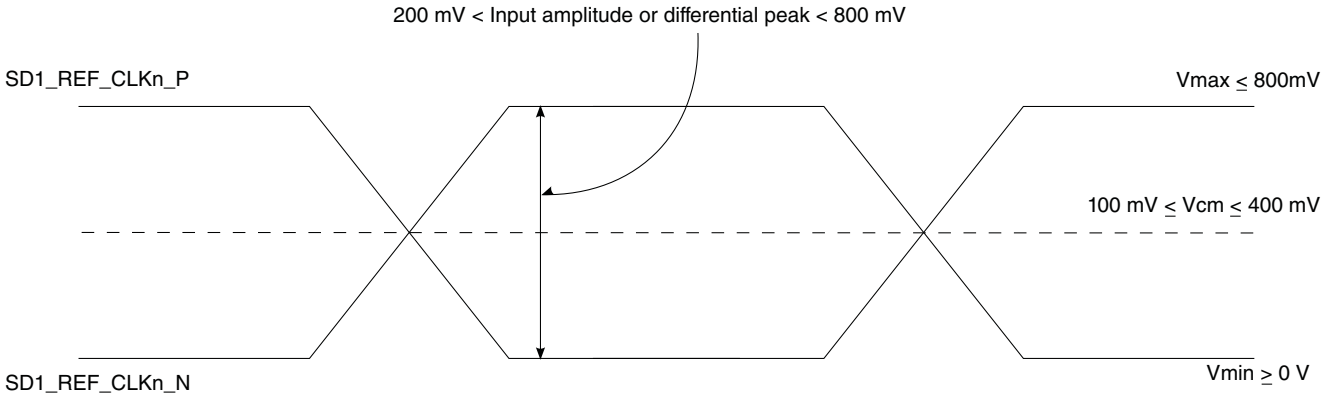
- The SerDes transceivers core power supply voltage requirements ($S1V_{DD}$) are as specified in Recommended operating conditions.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 3-57. Each differential clock input (SD1_REF_CLK*n*_P or SD1_REF_CLK*n*_N) has on-chip 50Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V ˜ 50 = 8 mA) while the minimum common mode input level is 0.1V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8V), such that each phase of the differential input has a single- ended swing from 0V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N inputs cannot drive 50Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.22.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

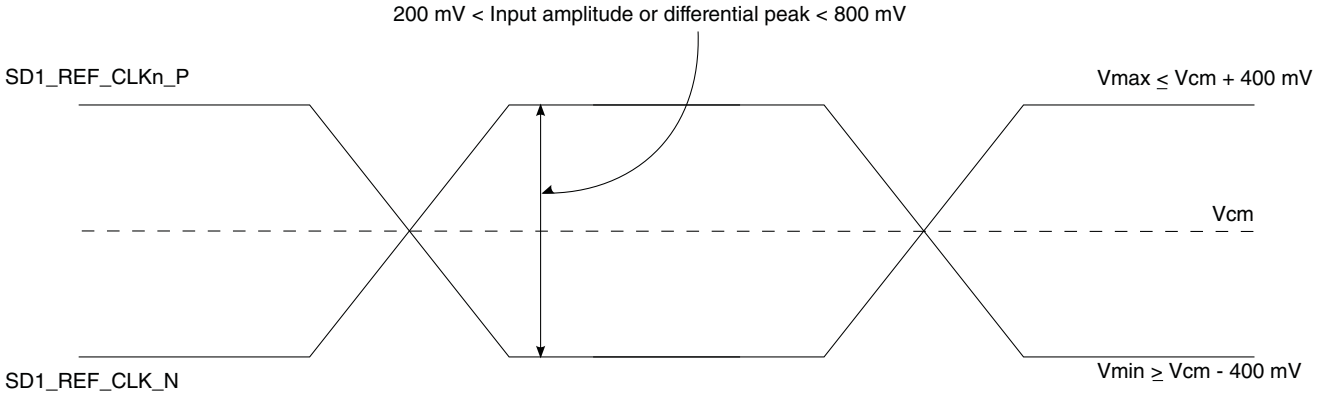
- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 3-58 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

Figure 3-58. Differential reference clock input DC requirements (external DC-coupled)



– For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*). Figure 3-59 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

Figure 3-59. Differential reference clock input DC requirements (external AC-coupled)



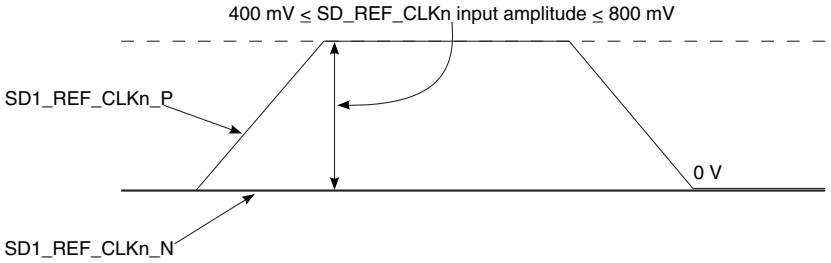
• Single-Ended Mode

– The reference clock can also be single-ended. The SD1_REF_CLKn_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to- peak (from V_{MIN} to V_{MAX}) with SD1_REF_CLKn_N either left unconnected or tied to ground.

– The SD1_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 3-60 shows the SerDes reference clock input requirement for single-ended signaling mode.

– To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD1_REF_CLK*n*_N) through the same source impedance as the clock input (SD1_REF_CLK*n*) in use.

Figure 3-60. Single-ended reference clock input DC requirements



3.22.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 5 Gb/s.

This includes PCI Express (2.5, 5 GT/s), SGMII (1.25Gbps), QSGMII (5Gbps). SerDes reference clocks to be guaranteed by the customer's application design.

Table 3-106. SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N input clock requirements ($S1V_{DD}n$ = 1.0V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/SD1_REF_CLKn_N frequency range	t_{CLK_REF}	–	100/125	–	MHz	2
SD1_REF_CLKn_P/SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	–300	–	300	ppm	3
SD1_REF_CLKn_P/SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	–100	–	100	ppm	4
SD1_REF_CLKn_P/SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLKn_P/SD1_REF_CLKn_N max deterministic peak–to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	–	–	42	ps	–
SD1_REF_CLKn_P/SD1_REF_CLKn_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	–	–	86	ps	6
SD1_REF_CLKn_P/SD1_REF_CLKn_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	–	–	3	ps RMS	7
SD1_REF_CLKn_P/SD1_REF_CLKn_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	–	–	3.1	ps RMS	7
SD1_REF_CLKn_P/SD1_REF_CLKn_N rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	–	4	V/ns	9
Differential input high voltage	V_{IH}	150	–	–	mV	5
Differential input low voltage	V_{IL}	–	–	–150	mV	5
Rising edge rate (SD1REF_CLKn_P) to falling edge rate (SD1_REF_CLKn_N) matching	Rise-Fall Matching	–	–	20	%	10, 11

Notes:
1. For recommended operating conditions, see Table 3-2.
2. **Caution:** Only 100 and 125 have been tested.In-between values do not work correctly with the rest of the system.
3. For PCI Express(2.5, 5 GT/s)
4. For SGMII, QSGMII
5. Measurement taken from differential waveform
6. Limits from PCI Express CEM Rev 2.0

7. For PCI Express-5 GT/s, per PCI Express base specification rev 3.0
8. Measured from –150 mV to +150 mV on the differential waveform (derived from SD1_REF_CLK*n*_P minus SD1_REF_CLK*n*_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 3-61.
9. Measurement taken from single-ended waveform
10. Matching applies to rising edge for SD1_REF_CLK*n*_P and falling edge rate for SD1_REF_CLK*n*_N. It is measured using a ±75 mV window centered on the median cross point where SD1_REF_CLK*n*_P rising meets SD1_REF_CLK*n*_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD1_REF_CLK*n*_P must be compared to the fall edge rate of SD1_REF_CLK*n*_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 3-62.

Figure 3-61. Differential measurement points for rise and fall time

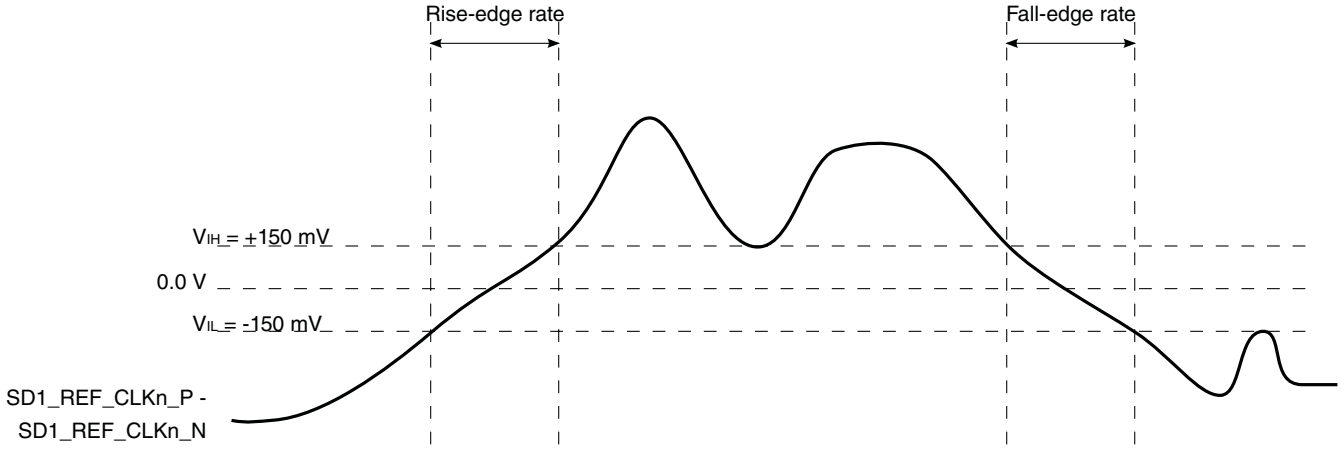
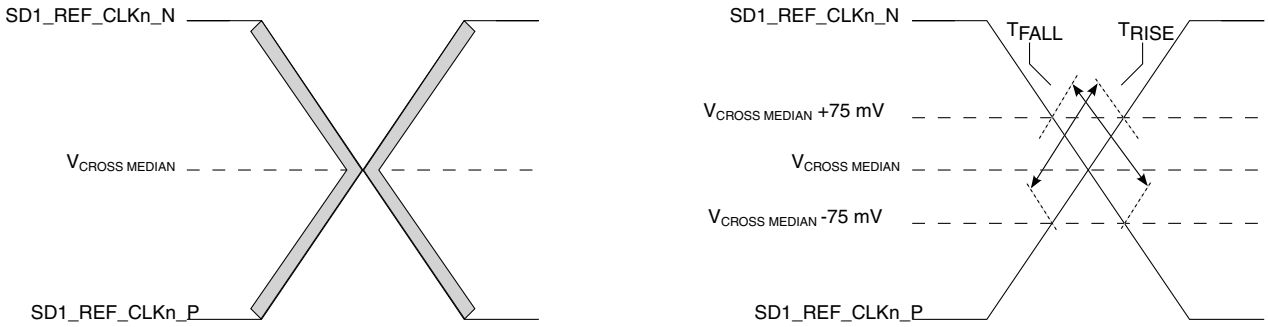


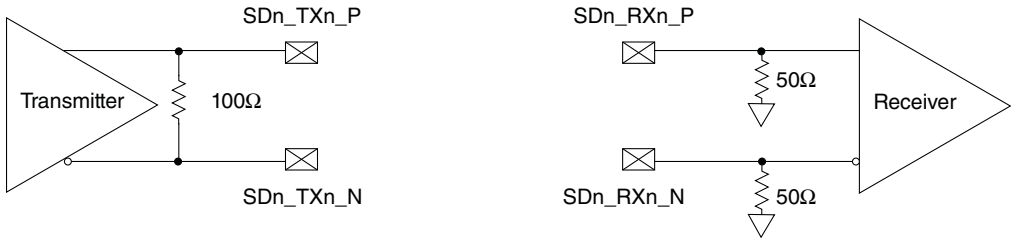
Figure 3-62. Single-ended measurement points for rise and fall time matching



3.22.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 3-63. SerDes transmitter and receiver reference circuits



The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Aurora interface
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.22.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

3.22.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.22.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.22.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 3-107. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 × I V_{TX-D+} – V_{TX-D-} I
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX- DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Note: 1. For recommended operating conditions, see Table 3-2.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 3-108. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 × I V_{TX-D+} - V_{TX-D-} I
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p}$ = 2 × I V_{TX-D+} - V_{TX-D-} I
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Note: 1. For recommended operating conditions, see Table 3-2.

3.22.4.3 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 3-109. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	–	–	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	–	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3-2.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 3-110. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	–	–	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	–	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$
						Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3-2.

3.22.4.4 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

3.22.4.4.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 3-111. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	–	–	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	–	–	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of
						sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	–	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in Figure 3-65 and measured over any 250 consecutive transmitter UIs.
2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 3-2.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 3-112. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	–	–	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	–	–	0.15	ps	–
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	–	3.0	–	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	–	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in Figure 3-65 and measured over any 250 consecutive transmitter UIs.
2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
3. For recommended operating conditions, see Table 3-2.

3.22.4.4.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 3-113. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications4

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	^{T}RX-EYE	0.4	–	–	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-}$ JITTER = 1 - ^{T}RX-EYE$^{= 0.6 UI.}$ See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	^{T}RX-EYE-MEDIAN- to-MAX-JITTER	–	–	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 3-65 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.
4. For recommended operating conditions, see Table 3-2.

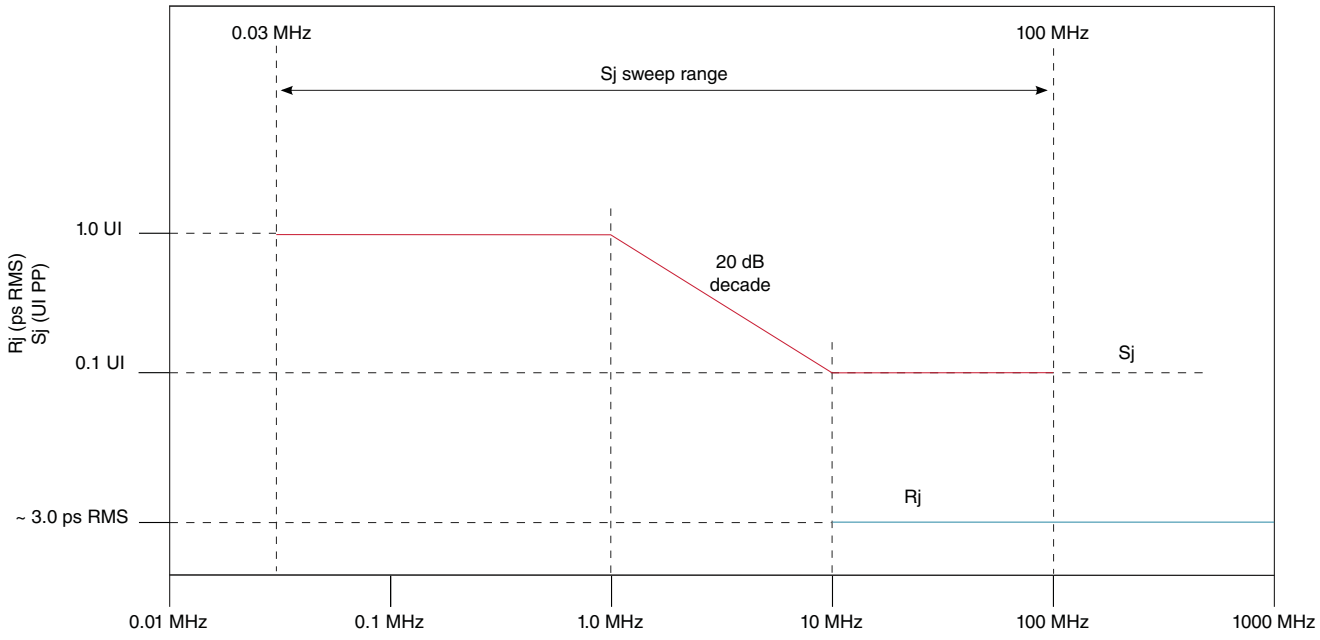
This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 3-114. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	–	–	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	–	–	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note: 1. For recommended operating conditions, see Table 3-2.

Figure 3-64. Swept sinusoidal jitter mask

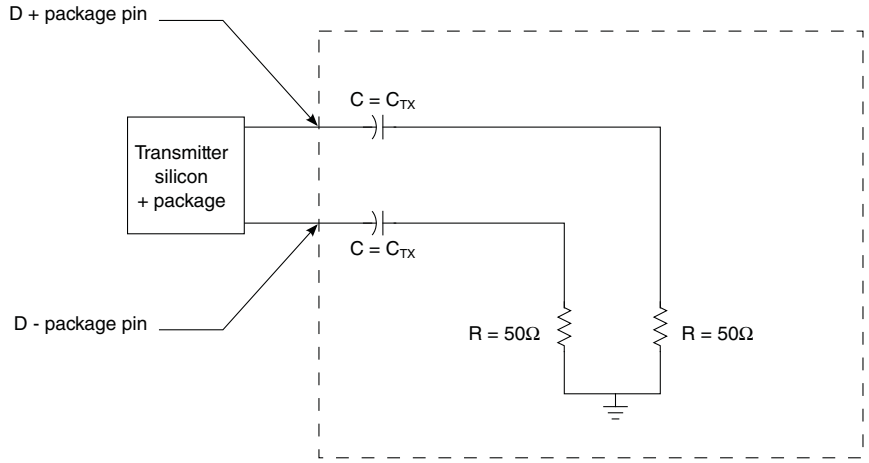


3.22.4.5 *Test and measurement load*

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE
The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/ board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

Figure 3-65. Test/measurement load



3.22.5 Aurora interface

This section describes the Aurora clocking requirements and its DC and AC electrical characteristics.

3.22.5.1 *Aurora clocking requirements for SD1_REF_CLKn_P and SD1_REF_CLKn_N*

For more information on these specifications, see SerDes reference clocks.

3.22.5.2 *Aurora DC electrical characteristics*

This section describes the DC electrical characteristics for the Aurora interface.

3.22.5.2.1 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 3-115. Aurora transmitter DC electrical characteristics (XV_{DD} = 1.35V) [1]

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω

Note: 1. For recommended operating conditions, see Table 3-2.

3.22.5.2.2 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for the Aurora interface.

Table 3-116. Aurora receiver DC electrical characteristics (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	–	1600	mV p-p	2
DC Differential receiver impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	3

Notes: 1. For recommended operating conditions, see Table 3-2.
2. Measured at receiver
3. DC Differential receiver impedance

3.22.5.3 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

3.22.5.3.1 Aurora transmitter AC timing specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 3-117. Aurora transmitter AC timing specifications1

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	–	–	0.17	UI p-p
Total jitter	J_T	–	–	0.35	UI p-p
Unit interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

Note: 1. For recommended operating conditions, see Table 3-2.

3.22.5.3.2 Aurora receiver AC timing specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 3-118. Aurora receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	–	–	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	–	–	0.55	UI p-p	1
Total jitter tolerance	J_T	–	–	0.65	UI p-p	1, 2
Bit error rate	BER	–	–	10^{-12}	–	–
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	–
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	–

Notes: 1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 3-14. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. For recommended operating conditions, see Table 3-2.

3.22.6 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

3.22.6.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.22.6.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 3-119. Gen1i/1m 1.5G transmitter DC specifications ($X1V_{DD}$ = 1.35V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Notes:
1. Terminated by 50 Ω load
2. DC impedance
3. For recommended operating conditions, see Table 3-2.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 3-120. Gen 2i/2m 3G transmitter DC specifications ($X1V_{DD}$ = 1.35V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	–	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	–

Notes:
1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 3-2.

3.22.6.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 3-121. Gen1i/1m 1.5 G receiver input DC specifications (SV_{DD} = 1.0V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	–

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance
3. For recommended operating conditions, see Table 3-2.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 3-122. Gen2i/2m 3 G receiver input DC specifications (SV_{DD} = 1.0V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	–	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance
3. For recommended operating conditions, see Table 3-2.

3.22.6.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

3.22.6.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock listed in this table are to be guaranteed by the customer's application design.

Table 3-123. SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/SD1_REF_CLKn_N frequency range	t_{CLK_REF}	–	100/125	–	MHz	1
SD1_REF_CLKn_P/SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	–350	–	+350	ppm	–
SD1_REF_CLKn_P/SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLKn_P/SD1_REF_CLKn_N cycle- to-cycle clock jitter (period jitter)	t_{CLK_CJ}	–	–	100	ps	2
SD1_REF_CLKn_P/SD1_REF_CLKn_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	–50	–	+50	ps	2, 3, 4

Notes:
1. **Caution:**Only 100 and 125MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform
6. For recommended operating conditions, see Table 3-2.

3.22.6.3 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 3-124. Gen1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Channel speed	t_{CH_SPEED}	–	1.5	–	Gbps	–
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	–
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	–	–	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	–	–	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	–	–	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	–	–	0.22	UI p-p	1

Notes: 1. Measured at transmitter output pins peak to peak phase variation, random data pattern

2. For recommended operating conditions, see Table 3-2.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 3-125. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Channel speed	t_{CH_SPEED}	–	3.0	–	Gbps	–
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	–
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	–	–	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	–	–	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	–	–	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	–	–	0.35	UI p-p	1

Notes: 1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern

2. For recommended operating conditions, see Table 3-2.

3.22.6.4 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 3-126. Gen 1i/1m 1.5G receiver AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	–
Total jitter data-data 5 UI	$U_{SATA\_RXTJ5UI}$	–	–	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	–	–	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	–	–	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	–	–	0.35	UI p-p	1

Notes: 1. Measured at receiver.

2. For recommended operating conditions, see Table 3-2.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 3-127. Gen 2i/2m 3G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	–
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	–	–	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	–	–	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXDJfB/500}$	–	–	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXDJfB/1667}$	–	–	0.35	UI p-p	1

Notes: 1. Measured at receiver

2. For recommended operating conditions, see Table 3-2.

4. HARDWARE DESIGN CONSIDERATIONS

4.1 System clocking

This section describes the PLL configuration of the chip.

4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There are two core cluster PLLs which generate a clock for each core cluster from the externally supplied SYSCLK input.
- Core cluster Group A PLL 1 and Core cluster group A PLL 2
- The frequency ratio between each of the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Core cluster to SYSCLK PLL ratio. The frequency for each core cluster is selected using the configuration bits as described in Table 4-4.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- Cluster group A generates an asynchronous clock for eSDHC SDR mode from CGA PLL1 or CGA PLL2. Described in eSDHC SDR mode clock select.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input. The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in DDR controller PLL ratios.
- SerDes block has 2 PLLs which generate a core clock from their respective
- externally supplied SD1_REF_CLK*n*_P/SD1_REF_CLK*n*_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in SerDes PLL ratio.
- When using Single Oscillator Source clocking mode, a single onboard oscillator can provide the reference clock (100MHz) to all the PLL's that is, Platform PLL, Core Cluster PLL's, DDR PLL, USB PLL and Serdes PLL's.

4.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 4-1. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1200 MHz		1400 MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	800	1200	800	1400	800	1500	MHz	1, 2
Core cluster frequency	400	1200	400	1400	400	1500	MHz	2
Platform clock frequency	300	500	300	600	300	600	MHz	1, 7
Memory bus clock frequency (DDR3L)	500	800	500	800	500	800	MHz	1, 3, 4
IFC clock frequency	–	100	–	100	–	100	MHz	5
FMAN	300	500	300	600	300	600	MHz	6

Notes:
1. **Caution:** The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies
2. The core cluster can run at cluster group PLL/1 and PLL/2. For the PLL/1 case, the minimum frequency is 800 MHz. With a minimum cluster group PLL frequency of 800 MHz, this results in a minimum allowable core cluster frequency of 400 MHz for PLL/2. Frequency provided to the e5500 cluster after any dividers must always be greater than or equal to the platform frequency. For the case of the minimum platform frequency = 400 MHz, the minimum core cluster frequency is 400 MHz.
3. The memory bus clock speed is half the DDR3L data rate.
4. The memory bus clock speed is dictated by its own PLL.
5. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV].
6. See the chip reference manual for more information.
7. 1200MHz bin cannot support Gen2, x4 PCIe. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.
8. "Single Oscillator Source" Reference clock mode supports differential reference clock pair frequency of 100MHz.

4.1.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 4-2. Memory bus clocking specifications

Characteristic		Min	Max	Unit	Notes
Memory bus clock frequency	DDR3L	500	800	MHz	1, 2, 3

Notes:
1. **Caution:** The platform clock to SYSCLK ratio and core to SYSCLK clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, and Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios, for ratio settings.
2. The memory bus clock refers to the chip's memory controllers' D1_MCK[0:1] and D1_MCK[0:1]_B output clocks, running at half of the DDR data rate.
3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios.

4.1.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock-frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 4-3. Platform to SYSCLK PLL ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
All Others	Reserved

4.1.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CGA_PLLn_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CGA_PLLn_CFG = 0b00.

This table lists the supported asynchronous core cluster to SYSCLK ratios.

Table 4-4. Core cluster PLL to SYSCLK ratios

Binary value of CGA_PLLn_RAT(n=1 or 2)	Core cluster:SYSCLK Ratio
00_0110	6:1
00_0111	7:1
00_1000	8:1
00_1001	9:1
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1
00_1111	15:1
01_0000	16:1
01_0010	18:1
01_0100	20:1
01_0110	22:1
01_1001	25:1
01_1010	26:1
01_1011	27:1
All others	Reserved

4.1.5 Core complex PLL select

The clock frequency of each core cluster is determined by the binary value of the RCW Configuration field Cn_PLL_SEL. These tables describe the selections available to each core cluster, where each individual core cluster can select a frequency from their respective tables.

NOTE

There is a restriction that requires that the frequency provided to the e5500 core cluster after any dividers must always be greater than half of the platform frequency. Special care must be used when selecting the /2 outputs of a cluster PLL in which this restriction is observed.

Table 4-5. Core cluster PLL select

Binary Value of Cn_PLL_SEL for n=1-4	Core cluster ratio
0000	CGA PLL1 /1
0001	CGA PLL1 /2
0100	CGA PLL2 /1
0101	CGA PLL2 /2
All Others	Reserved

4.1.6 DDR controller PLL ratios

The DDR memory controller operates asynchronous to the platform.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 4-6. DDR clock ratio

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
00_1000	8:1	1066
00_1010	10:1	1333
00_1011	11:1	1465
00_1100	12:1	1600
00_1101	13:1	1300
00_1110	14:1	1400
00_1111	15:1	1500
01_0000	16:1	1600
1_0100	20:1	1333
1_1000	24:1	1600
All Others	Reserved	–

4.1.7 SerDes PLL ratio

The clock ratio between each of the two SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLKn_N inputs is determined by a set of RCW Configuration fields-SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_*_S1 as shown in this table.

Table 4-7. Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S1	Legal setting for SRDS_PLL_REF_CLK_SEL_S1	Legal setting for SRDS_DIV_*_S1	Notes
High-speed serial interfaces					
PCI Express 2.5 Gbps (doesn't negotiate upwards)	100 MHz	Any PCIe	0b0: 100 MHz	2b10: 2.5 G	1
	125 MHz		0b1: 125 MHz		1
PCI Express 5 Gbps (can negotiate up to 5 Gbps)	100 MHz	Any PCIe	0b0: 100 MHz	2b01: 5.0 G	1
	125 MHz		0b1: 125 MHz		1
SATA (1.5 or 3 Gbps)	100 MHz	Any SATA	0b0: 100 MHz	Don't care	2
	125 MHz		0b1: 125 MHz		
Debug (2.5 Gbps)	100 MHz	Aurora @ 2.5/5 Gbps	0b0: 100 MHz	0b1: 2.5 G	–
	125 MHz		0b1: 125 MHz		–
Debug (5 Gbps)	100 MHz	Aurora @ 2.5/5 Gbps	0b0: 100 MHz	0b0: 5.0 G	–
	125 MHz		0b1: 125 MHz		–
Networking interfaces					
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps 1000Base-KX @ 1.25 Gbps	0b0: 100 MHz	Don't care	–
	125 MHz		0b1: 125 MHz		–
QSGMII (5.0 Gbps)	100 MHz	Any QSGMII	0b0: 100 MHz	0b0: 5.0 G	–
	125 MHz		0b1: 125 MHz		–

Notes:
1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface such as SATA, SGMII, QSGMII, 1000Base-KX, is used concurrently on the same SerDes PLL, spread-spectrum clocking is not permitted.
2. SerDes lanes configured as SATA initially operate at 3.0 Gbps. 1.5 Gbps operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rate.

4.1.8 eSDHC SDR mode clock select

The eSDHC SDR mode is asynchronous to the platform.

This table describes the clocking options that may be applied to the eSDHC SDR mode. The clock selection is determined by the binary value of the RCW Clocking Configuration field HWA_CGA_M1_CLK_SEL.

Table 4-8. eSDHC SDR mode clock select

Binary value of HWA_CGA_M1_CLK_SEL	eSDHC SDR mode frequency[1]
0b000	Reserved
0b001	Cluster group A PLL 1/1
0b010	Cluster group A PLL 1/2
0b011	Cluster group A PLL 1/3
0b100	Cluster group A PLL 1/4
0b101	Reserved
0b110	Cluster group A PLL 2/2
0b111	Cluster group A PLL 2/3

Notes:
1. For asynchronous mode, max frequency, see table "Processor clocking specifications" in the chip reference manual.
2. For SDR104 and HS200 modes, CGA1 PLL should be set to provide a minimum of 1200MHz.
3. For SDR50 mode, Cluster PLL should be set to provide a minimum of 600MHz

4.1.9 Frequency options

This section discusses interface frequency options.

4.1.9.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 4-9. SYSCLK and core cluster frequency options

Core cluster: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	**66.67**	**100.00**	**125.00**	**133.33**
	Core cluster Frequency (MHz)[1]				
6:1					800
7:1				875	933
8:1			800	1000	1067
9:1			900	1125	1200
10:1			1000	1250	1333
11:1			1100	1375	
12:1		800	1200	1500	
13:1	832	867	1300		
14:1	896	933	1400		
15:1	960	1000	1500		
16:1	1024	1067			
18:1	1152	1200			
20:1	1280	1333			
21:1	1344	1400			

Notes: 1. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)

2. When using Single Source clocking only 100MHz input is available.

4.1.9.2 *SYSCLK and platform frequency options*

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 4-10. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	**66.67**	**100.00**	**125.00**	**133.33**
	Platform Frequency (MHz)[(1)]				
3:1			300	375	400
4:1			400	500	533
5:1	320	333	500		
6:1	384	400	600		
7:1	448	467			
8:1	512	533			
	Platform Frequency (MHz)[(1)]				
9:1	576	600			

Notes: 1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

2. When using Single source clocking, only 100MHz options are valid

4.1.9.3 *DDRCLK and DDR data rate frequency options*

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 4-11. DDRCLK and DDR data rate frequency options

DDR data rate: DDRCLK Ratio	DDRCLK (MHz)				
	64.00	**66.67**	**100.00**	**125.00**	**133.33**
	DDR Data Rate (MT/s)[1]				
8:1				1000	1066
10:1			1000	1250	1333
11:1			1100	1375	1465
12:1			1200	1500	1600
13:1			1300		
14:1			1400		
15:1		1000	1500		
16:1	1024	1067	1600		
20:1	1280	1333			
24:1	1536	1600			

Notes: 1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed)

2. When using Single Source clocking, only 100MHz options are available.

4.1.9.4 *SYSCLK and eSDHC High Speed modes frequency options*

These table shows the expected frequency options for SYSCLK and eSDHC High Speed modes.

Table 4-12. SYSCLK and eSDHC High Speed mode frequency options (clocked by CGA PLL1 /1)

Core cluster: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Resultant Frequency (MHz)[1]				
9:1					1200
12:1			1200		
18:1	1152	1200			

Notes: 1. Resultant frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)

2. For Low speed operation, eSDHC is clocked from Platform PLL and does not use CGA PLL.

4.1.9.5 *Minimum platform frequency requirements for high-speed interfaces*

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

Figure 4-1. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 4-2. Gen 2 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use. For instance, if two x4 PCIe Gen2 ports are in use, 527MHz platform frequency is needed to support by using Gen 2 equation (527 × 4 / 4, not 527 × 4 × 2 / 4).

NOTES

1. Platform needs to run at a minimum frequency of 527MHz for PEX in Gen2 speed with x4 link width.
2. Platform needs to run at a minimum frequency of 400MHz for PEX in Gen2 speed.

4.2 Power supply design

4.2.1 Core and platform supply voltage filtering

The V_{DD}, V_{DDC} supply is normally derived from a high current capacity linear or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, TELEDYNE e2v recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than 1.0V+50 mV (negative transient undershoot should comply with specification of 1.0V-30mV) for current steps of up to 10A with a slew rate of 12 A/us.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see Decoupling recommendations for further decoupling recommendations.

4.2.2 PLL power supply filtering

Each of the PLLs described in System clocking is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_D1 and AV_{DD}_SD1_PLLn). AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_CGA2 and AV_{DD}_D1 voltages must be derived directly from a 1.8V voltage source through a low frequency filter scheme. AV_{DD}_SD1_PLLn voltages must be derived directly from the $X1V_{DD}$ source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 4-3, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

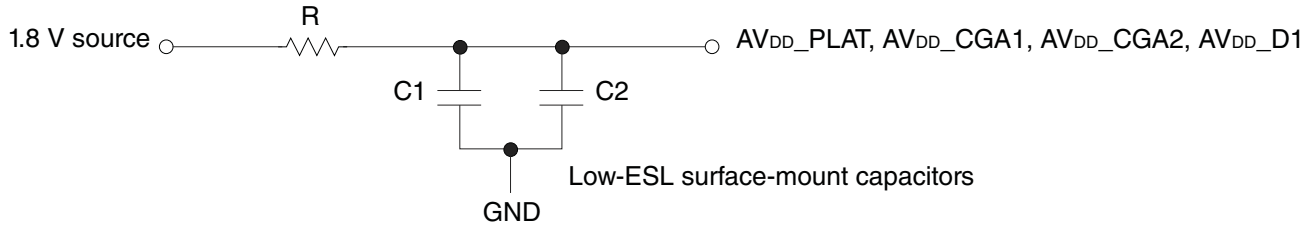
This figure shows the PLL power supply filter circuit. Where:

- R = 5Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE
A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

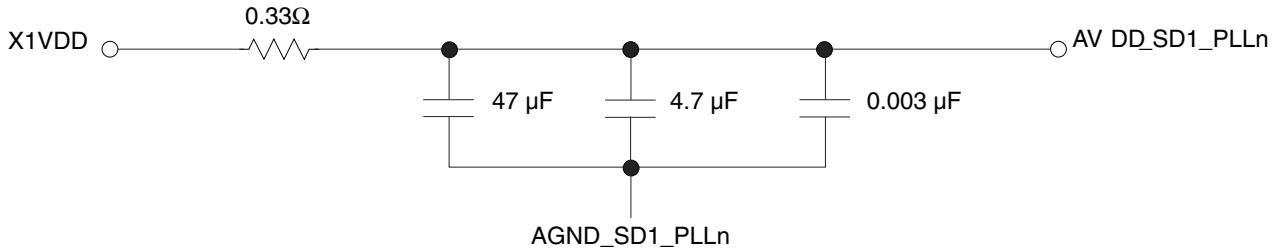
NOTE
Voltage for AVDD is defined at the input of the PLL supply filter and not the pin of AVDD.

Figure 4-3. PLL power supply filter circuit



The AV_{DD}_SD1_PLLn signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 4-4. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SD1_PLLn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SD1_PLLn balls. The 0.003-µF capacitors closest to the balls, followed by a 4.7-µF and 47-µF capacitor, and finally the 0.33Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SD*1*_PLL*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

Figure 4-4. SerDes PLL power supply filter circuit



Note the following:

- AV_{DD}_SD*n*_PLL*n* should be a filtered version of X*n*V_{DD}.
- Signals on the SerDes interface are fed from the $X1V_{DD}$ power plane.
- Voltage for AV_{DD}_SD1_PLLn is defined at the PLL supply filter and not the pin of AV_{DD}_SD1_PLL*n*.
- A 47-µF 0805 XR5 or XR7, 4.7-µF 0603, and 0.003-µF 0402 capacitor are recommended. The size and material type are important. A 0.33-Ω ± 1% resistor is recommended.
- There needs to be dedicated analog ground, AGND_SD1_PLL*n* for each AV_{DD}_SD1_PLL*n* pin up to the physical local of the filters themselves.

4.2.3 $S1V_{DD}$ power supply filtering

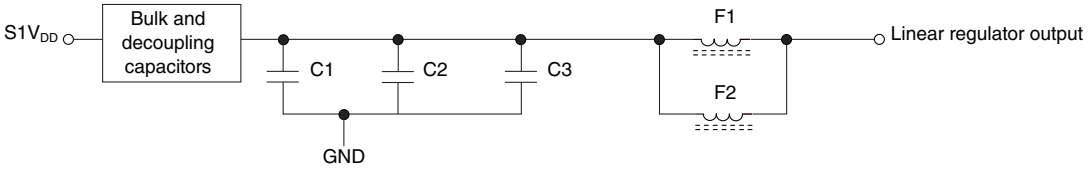
$S1V_{DD}$ should be supplied by a linear regulator.

An example solution for $S1V_{DD}$ filtering, is illustrated in Figure 4-5. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ .0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ .0.5 nH
- F1 and F2 = 120Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 4-5. SV_{DD} power supply filter circuit



Note the following:

- Refer to Power-on ramp rate, for maximum $S1V_{DD}$ power-up ramp rate.
- There needs to be enough output capacitance or a soft start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low noise dedicated switching regulator can also be used. 10 mVp-p, 50kHz - 500MHz is the noise goal.

4.2.4 $X1V_{DD}$ power supply filtering

$X1V_{DD}$ may be supplied by a linear regulator or sourced by a filtered $G1V_{DD}$. Systems may design in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended.

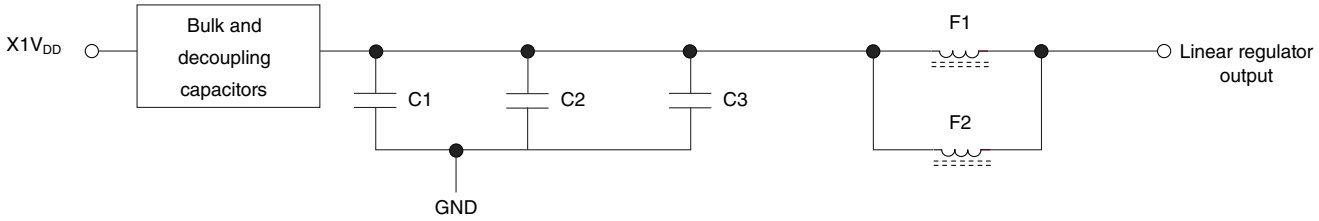
An example solution for $X1V_{DD}$ filtering, where $X1V_{DD}$ is sourced from a linear regulator, is illustrated in Figure 4-6. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ .0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ .0.5 nH
- F1 and F2 = 120Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Note the following:

Figure 4-6. $X1V_{DD}$ power supply filter circuit



- See Power-on ramp rate for maximum $X1V_{DD}$ power-up ramp rate.
- There needs to be enough output capacitance or a soft-start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low-noise, dedicated switching regulator can be used. 10 mVp-p, 50 kHz –500 MHz is the noise goal.

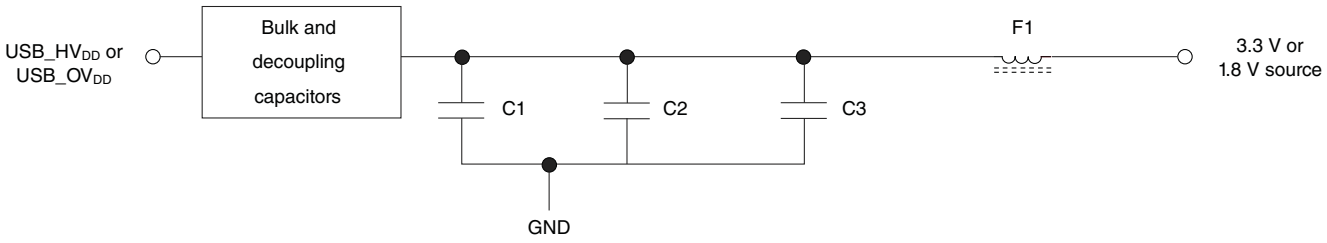
4.2.5 USB_HVDD and USB_OVDD power supply filtering

USB_HV_{DD} and USB_OV_{DD} must be sourced by a filtered 3.3V and 1.8V voltage source using a star connection. An example solution for USB_HV_{DD} and USB_OV_{DD} filtering, where USB_HV_{DD} and USB_OV_{DD} are sourced from a 3.3V and 1.8V voltage source, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 = 120Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 4-7. USB_HV_{DD} and USB_OV_{DD} power supply filter circuit



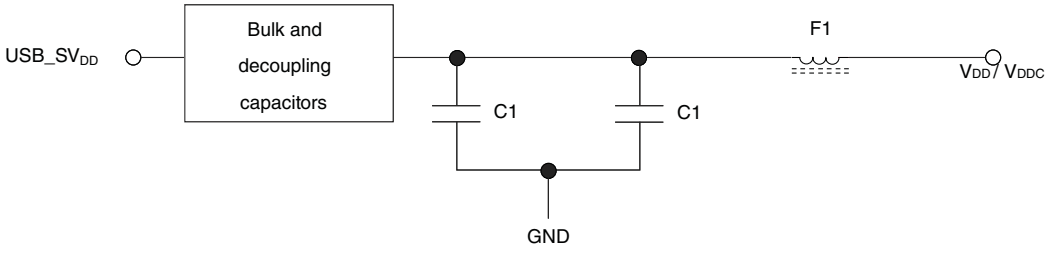
4.2.6 USB_SV_{DD} power supply filtering

USB_SV_{DD} must be sourced by a filtered V_{DD} or V_{DDC}using a star connection. An example solution for USB_SV_{DD} filtering, where USB_SV_{DD} is sourced from V_{DD}, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)
- F1 = 120Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 4-8. USB_SV_{DD} power supply filter circuit



4.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, V_{DDC}, CV_{DD}, OnV_{DD}, DV_{DD}, EV_{DD}, GnV_{DD}, and LnV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, CV_{DD}, OnV_{DD}, DV_{DD}, EV_{DD}, GnV_{DD}, LnV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0201 sizes.

As presented in Core and platform supply voltage filtering, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, V_{DDC} and other planes (for example, CV_{DD}, OnV_{DD}, DV_{DD}, EV_{DD}, GnV_{DD}, and LnV_{DD}), to enable quick recharging of the smaller chip capacitors.

4.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power ($S1V_{DD}$ and $X1V_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

NOTE

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 1 × 0.1-µF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor for example a 10-µF, low ESR SMT tantalum or ceramic and a higher bulk capacitor for example a 100µF - 300-µF low ESR SMT tantalum or ceramic capacitor.

4.5 Connection recommendations

The following is a list of connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low inputs should be tied to V_{DD}, OnV_{DD}, DV_{DD}, GnV_{DD}, EV_{DD}, CV_{DD} and LnV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, OnV_{DD}, DV_{DD}, GnV_{DD}, LnV_{DD} , EV_{DD} , CV_{DD} and GND pins of the device.
- The TEST_SEL_B pin must be pulled to $O1V_{DD}$ through a 100-ohm to 1k-ohm resistor for QT1040 and tied to ground for 2 core QT1020.
- The chip has temperature diodes on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). If a temperature diode monitoring device is not connected, these pins may be connected to test points or grounded.

4.5.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 4-10. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 4-10 allows the COP port to independently assert PORESET_B or TRST_B, while ensuring that the target can drive PORESET_B as well.

The COP interface has a standard header, shown in Figure 4-9, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 4-9 is common to all known emulators.

4.5.1.1 *Termination of unused signals*

If the JTAG interface and COP header will not be used, TELEDYNE e2v recommends the following connections:

- TRST_B should be tied to PORESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. TELEDYNE e2v recommends that the COP header be designed into the system as shown in Figure 4-10. If this is not possible, the isolation resistor will allow future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS or TDO.

Figure 4-9. Legacy COP Connector Physical Pinout

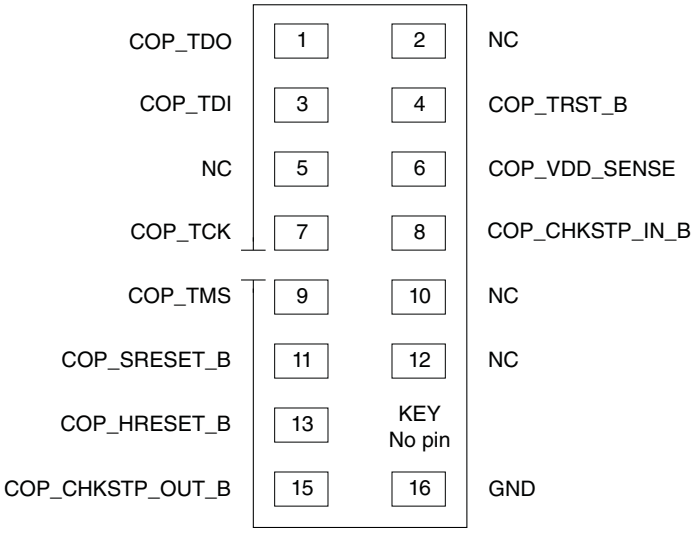
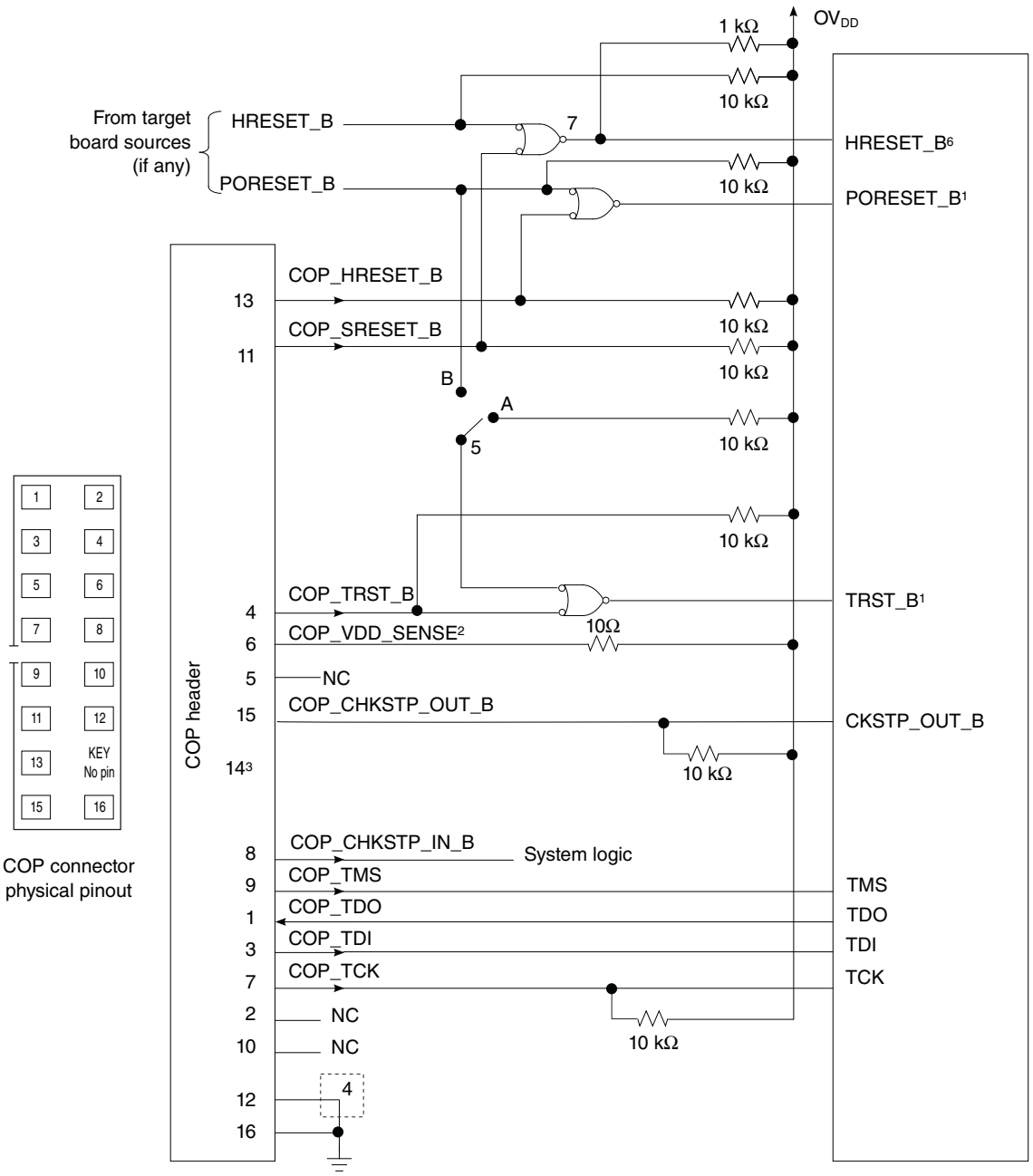


Figure 4-10. Legacy JTAG Interface Connection



Notes:
1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 10Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

6. Asserting HRESET_B causes a hard reset on the device
7. This is an open-drain output gate.

4.5.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in the figures below. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TELEDYNE e2v recommends that the Aurora 34 pin duplex connector be designed into the system as shown in Figure 4-11 or the 70 pin duplex connector be designed into the system as shown in Figure 4-12.

If the Aurora interface will not be used, TELEDYNE e2v recommends the legacy COP header be designed into the system as described in.

Figure 4-11. Aurora 34 pin connector duplex pinout

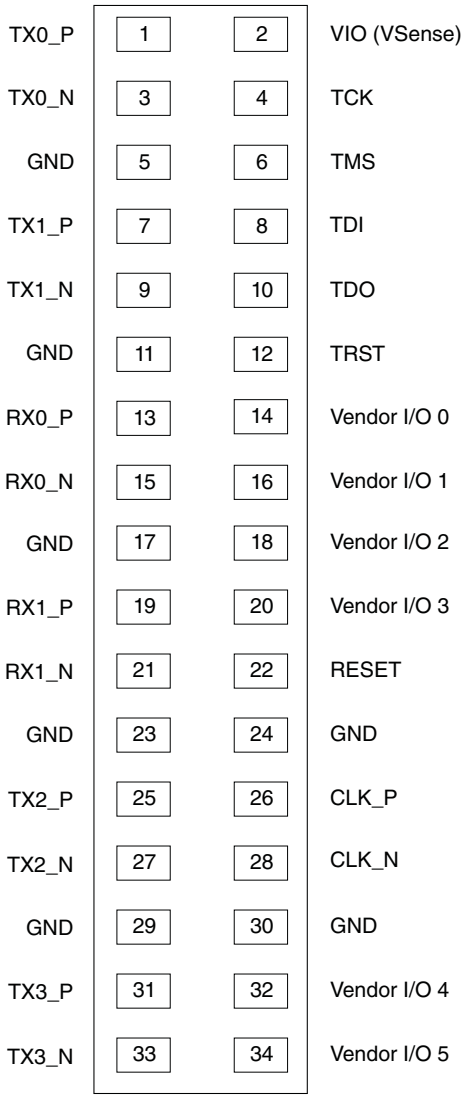


Figure 4-12. Aurora 70 pin connector duplex pinout

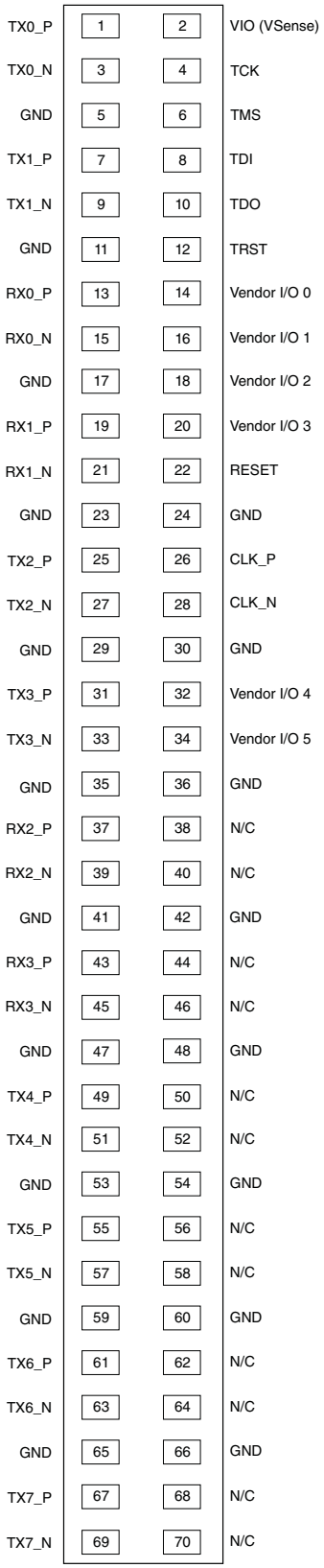
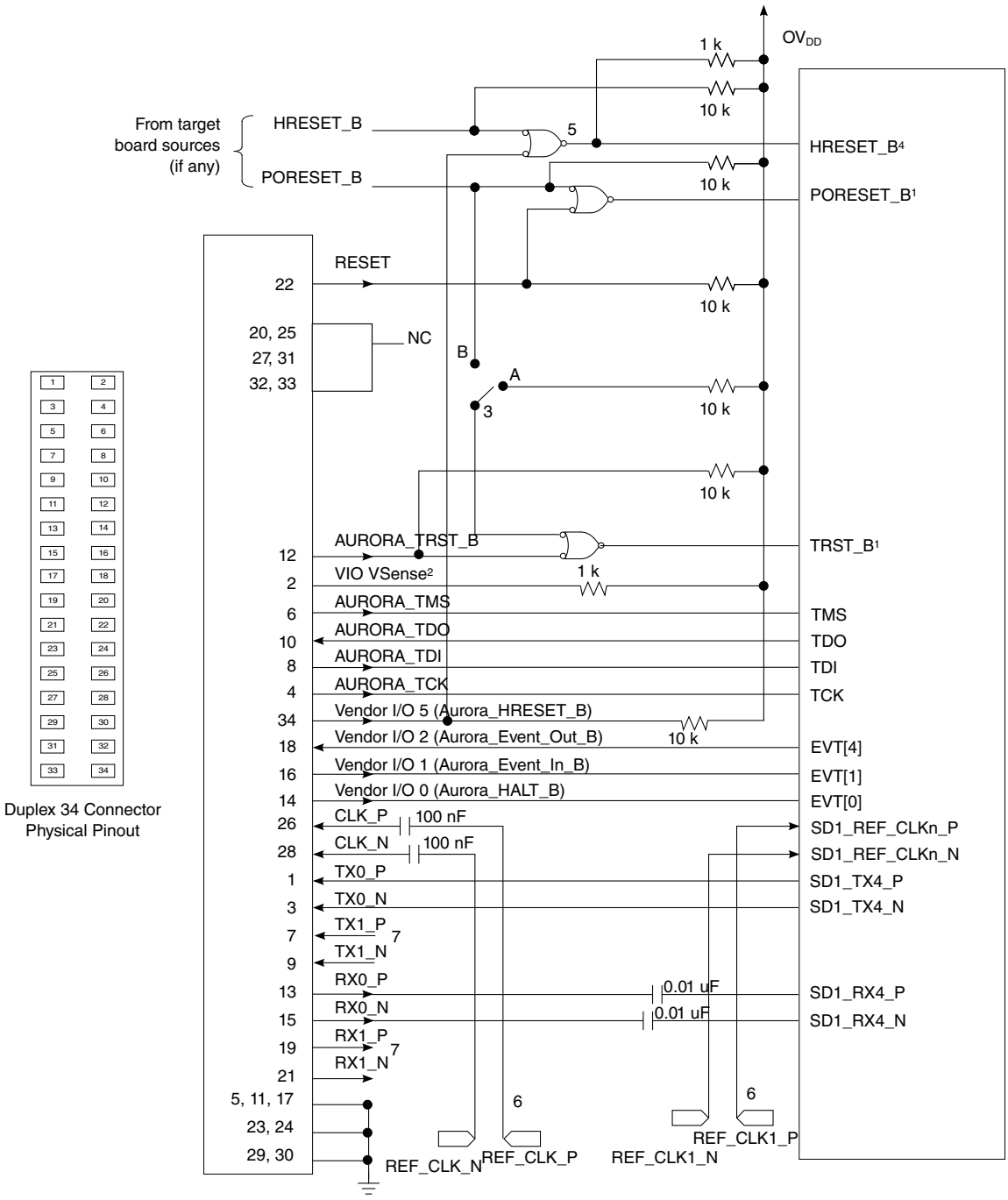


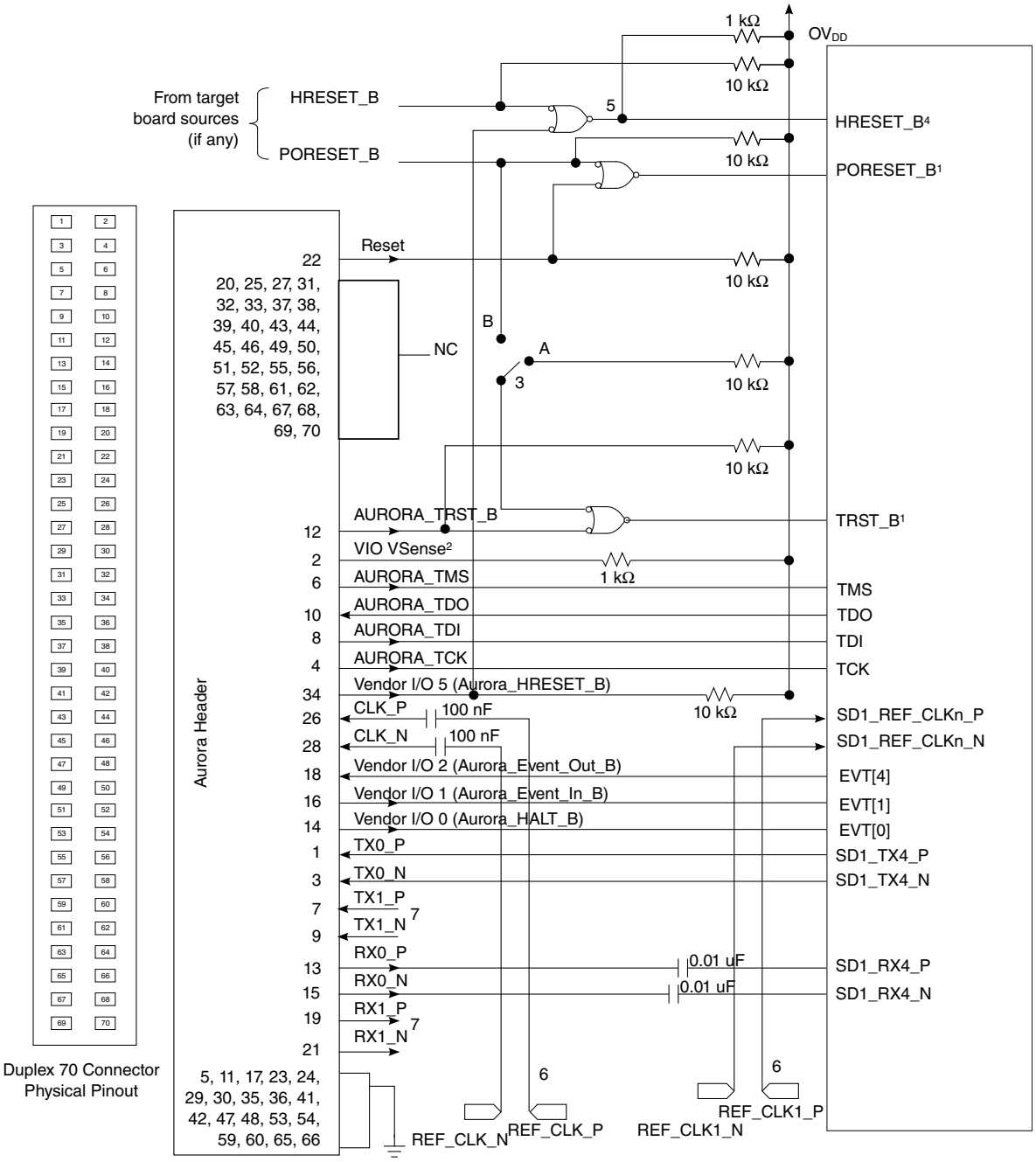
Figure 4-13. Aurora 34 pin connector duplex interface connection



Notes:
1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device.

5. This is an open-drain output gate.
6. REF_CLK_P/REF_CLK_N and REF_CLK1_P/REFCLK1_N are buffered clocks from the same common source.
7. RX1_P/RX1_N and TX1_P/TX1_N can be left floating at Aurora Header

Figure 4-14. Aurora 70 pin connector duplex interface connection



Notes:
1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.

3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device
5. This is an open-drain output gate.
6. REF_CLK_P/REF_CLK_N and REF_CLK1_P/REFCLK1_N are buffered clocks from the same common source.
7. RX1_P/RX1_N and TX1_P/TX1_N can be left floating at Aurora Header

4.5.3 Guidelines for high-speed interface termination

4.5.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that $S1V_{DD}$, $X1V_{DD}$ and AVDD_SD1_PLL1 must remain powered.

For AVDD_SD1_PLL1, it must be connected to $X1V_{DD}$ through a zero ohm resistor (instead of filter circuit shown in Figure 4-4).

The following pins must be left unconnected:

- SD1_TX[7:0]_P
- SD1_TX[7:0]_N
- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

The following pins must be connected to S1GND:

- SD1_REF_CLK1_P, SD1_REF_CLK2_P
- SD1_REF_CLK1_N, SD1_REF_CLK2_N

It is recommended for the following pins to be connected to S1GND:

- SD1_RX[7:0]_P
- SD1_RX[7:0]_N

It is possible to disable SerDes module by disabling all PLLs associated with it. SerDes is disabled as follows:

- SRDS_PLL_PD_S1 = 2’b11 (both PLLs configured as powered down, all data lanes selected by the protocols defined in SRDS_PRTCL_S1 associated to the PLLs are powered down as well)
- SRDS_PLL_REF_CLK_SEL_S1 = 2’b00
- SRDS_PRTCL_S1 = 2 (no other values permitted when both PLLs are powered down

4.5.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both $S1V_{DD}$ and $X1V_{DD}$ must remain powered.

If any of the PLLs are un-used, the corresponding AVDD_SD1_PLL1 must be connected to $X1V_{DD}$ through a zero ohm resistor (instead of filter circuit shown in Figure 4-4).

The following unused pins must be left unconnected:

- SD1_TX[7:0]_P
- SD1_TX[7:0]_N

The following unused pins must be connected to S1GND:

- SD1_REF_CLK[1:2]_P, SD1_REF_CLK[1:2]_N (If entire SerDes unused) It is recommended for the following unused pins to be connected to S1GND:
- SD1_RX[7:0]_P
- SD1_RX[7:0]_N

In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. A module is disabled when both its PLLs are turned off.

Unused lanes must be powered down through the SRDSx Lane m General Control Register 0 (SRDSxLNmGCR0) as follows:

- SRDSxLNmGCR0[RRST] = 0
- SRDSxLNmGCR0[TRST] = 0
- SRDSxLNmGCR0[RX_PD] = 1
- SRDSxLNmGCR0[TX_PD] = 1

Note that in the case where the SerDes pins are connected to slots, it is acceptable to have these pins unterminated when unused.

4.5.4 USB controller connections

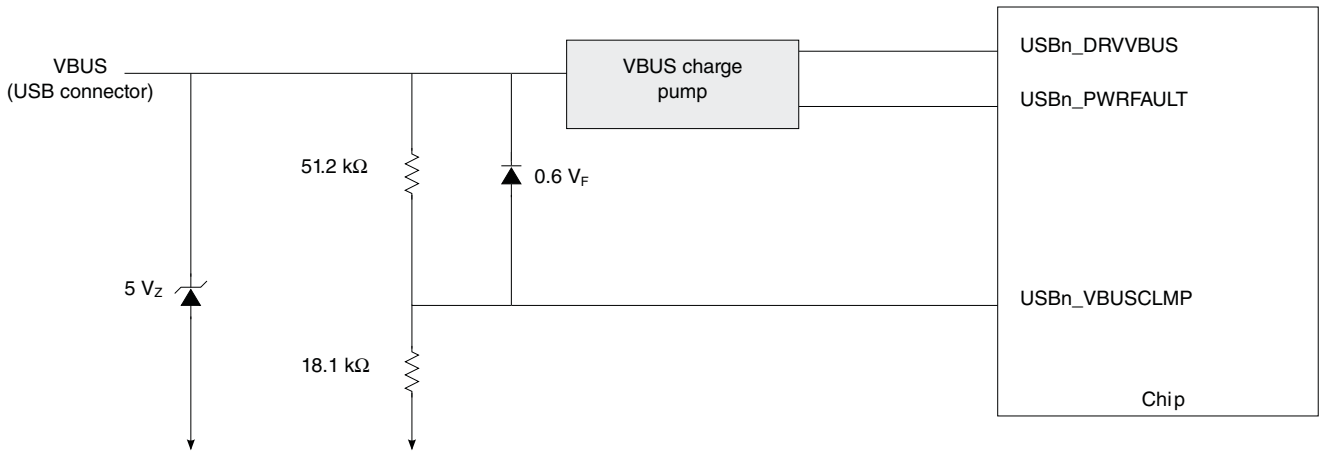
This section details the hardware connections required for the USB controllers.

4.5.4.1 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are:

- Both resistors require 1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5V-5.25V.
- The 0.6V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8V. If the USB PHY does not support OTG mode, this diode can be removed from the schematic or made a DNP component.

Figure 4-15. Divider network at VBUS



4.6 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 4-13. Package thermal characteristics[5]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	28	°C/W	(1)(2)
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	19	°C/W	(1)(3)
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	22	°C/W	(1)(2)
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	15	°C/W	(1)(2)
Junction to board	–	$R_{\Theta JB}$	9	°C/W	(3)
Junction to case top	–	$R_{\Theta JCtop}$	<0.1	°C/W	(4)

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. See Thermal management information, for additional details.

This table provides the thermal resistance with heat sink in open flow

Table 4-14. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
53 × 53 × 25 mm Pin Fin	Natural Convection	6.6
	0.5 m/s	3.9
	1 m/s	2.9
	2 m/s	2.5
	4 m/s	2.2
35x31x23 mm Pin Fin	Natural Convection	8.7
	0.5 m/s	5.0
	1 m/s	4.2
	2 m/s	3.6
	4 m/s	3.1
30x30x9.4 mm Pin Fin	Natural Convection	12.1
	0.5 m/s	8.2
	1 m/s	6.4
	2 m/s	5.0
	4 m/s	4.1
43x41x16.5 mm Pin Fin	Natural Convection	8.9
	0.5 m/s	5.4
	1 m/s	4.2
	2 m/s	3.3
	4 m/s	2.7

Notes: 1. Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.

2. Simulation details:
Substrate metal thicknesses: 0.015, 0.025 mm
Substrate core thickness: 0.4 mm

4.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local TELEDYNE e2v sales office.

4.8 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using 3 current measurements, where up to 1.5kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode: Operating range:
10 – 230 µA

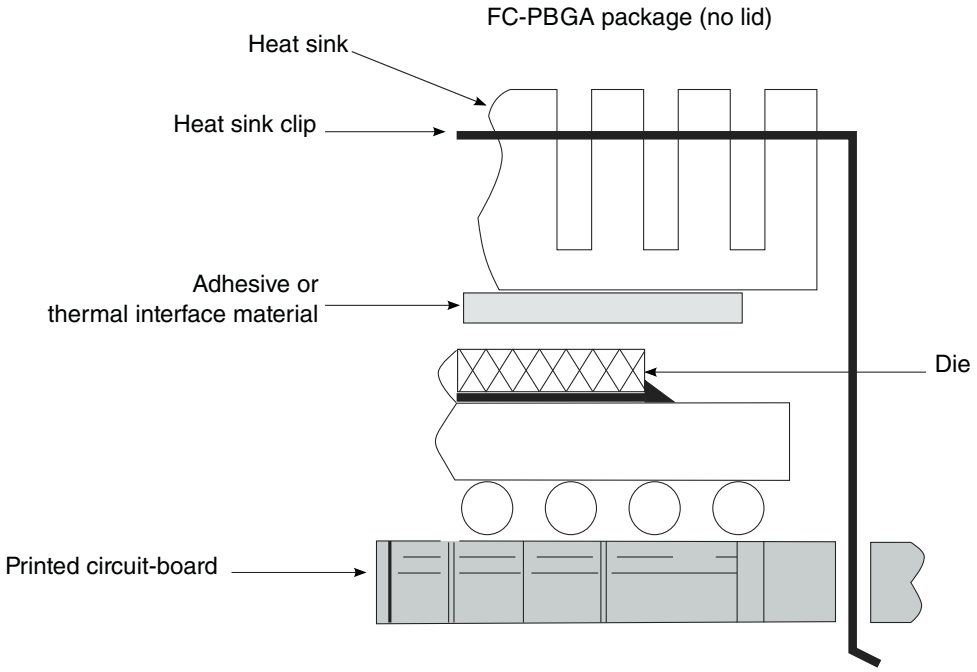
Ideality factor over 13.5 – 220 µA; Temperature range 80×C – 105×C: n = 1.004 ± 0.008

4.9 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 4-16. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (65 Newton).

Figure 4-16. Package exploded, cross-sectional view-FC-PBGA (no lid)



The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

For additional information regarding thermal management of lid-less flip-chip packages, refer to application note AN4871, "Assembly Handling and Thermal Solutions for Lidless Flip Chip Ball Grid Array PackInternal package conduction resistance

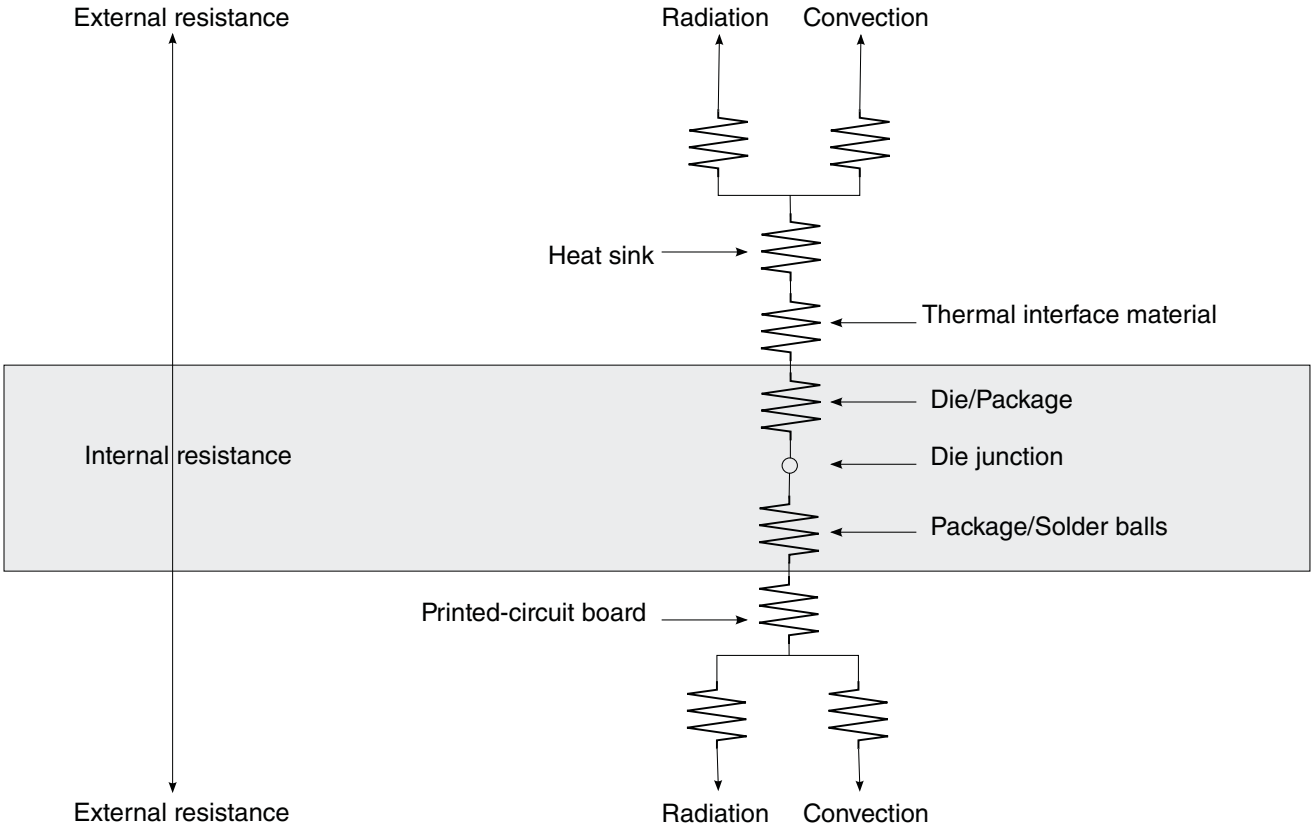
For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

RadiationConvection

Figure 4-17. Package with heat sink mounted to a printed-circuit board



(Note the internal versus external package resistance)

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

4.9.1 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 4-16).

The system board designer can choose among several types of commercially-available thermal interface materials.

5. PACKAGE INFORMATION

5.1 Package parameters for the FC-PBGA

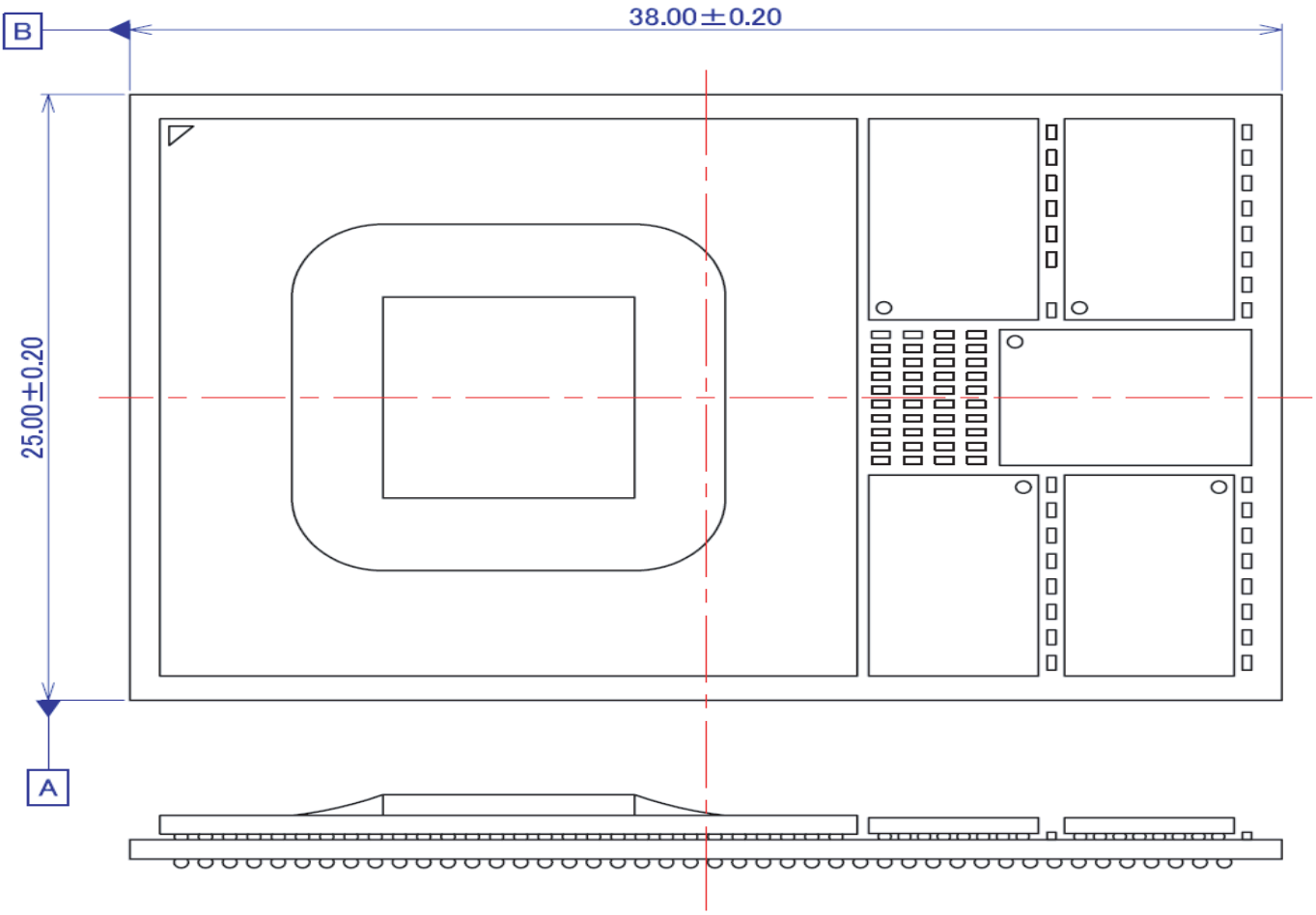
The package parameters are as provided in the following list. The package type is 23 mm × 23 mm, 780 flip-chip, plastic-ball, grid array (FC-PBGA).

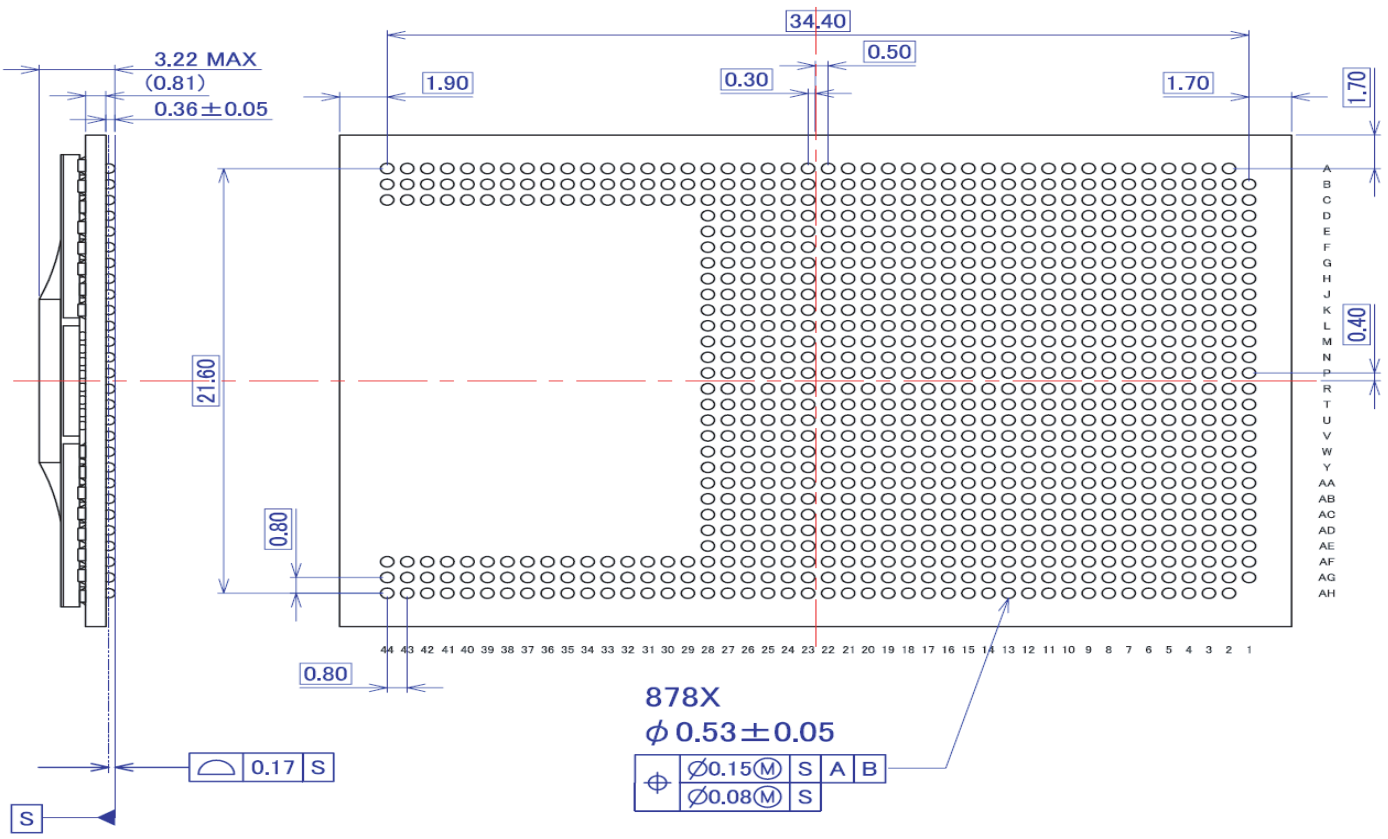
- Package outline - 25 mm × 38 mm
- Interconnects - 878
- Ball Pitch - 0.8 mm
- Ball Diameter (typical) - 0.45 mm
- Solder Balls - 96.5% Sn, 3% Ag, 0.5% Cu
- Module height - TBC

5.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

Figure 5-1. Mechanical dimensions of the FC-PBGA





Notes: 1. All measurement in millimeters

2. Unless otherwise specified :
   Tolerance : decimal = +/- 0.1mm
   Angular ±1°

6. SECURITY FUSE PROCESSOR

This chip implements the Qormino platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8V to the PROG_SFP pin per Power sequencing. PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering PROG_SFP are shown in Figure 3-3. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3-2.

NOTE
Users not implementing the Qormino platform's Trust Architecture features should connect PROG_SFP to GND.

7. ORDERING INFORMATION

Contact your local TELEDYNE e2v sales office or regional marketing team for order information.

Table 7-1. Ordering Information

Generation	Platform	Number of virtual cores	Derivatives	Temperature range	Encryption	Package Type	CPU Speed	DDR Data Rate	Memory size	Memory type	Product Revision
QT(X) = 28 nm Qormino	1	04 = 4 virtual cores	0 = First product	V = -40/110 M = -55/125 C = 0/105	E = SEC present N = SEC not present	7 = MCM C4/C5 Pbfree 3 = SnPb	M = 1200 MHz P = 1400 MHz	K = 1000 MT/s M = 1200 MT/s N = 1333 MT/s Q = 1600 MT/s	1 = 1GB	3 = DDR3L	A = Rev 1.0

Notes: 1. For availability of the different versions, contact your local TELEDYNE e2v sales office.

2. The letter × in the part number designates a "Prototype" product that has not been qualified by TELEDYNE e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

8. REVISION HISTORY

This table provides revision history for this document.

Table 8-1. Revision History

Rev. No	Date	Substantive Change(s)
1183B	04/2017	Added a new Section 3.5.2 ”DDR3L power consumption” on page 54 Removed duplicated pins in Table 2-1 .
1183A	01/2016	Initial revision

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