TELEDYNE e2v HIREL ELECTRONICS
Everywhereyoulook™

Peregrine Semiconductor

July 31, 2020

Product Specification
PE97640

Radiation Tolerant UltraCMOS® Delta-Sigma Modulated Fractional-N Frequency Synthesizer for Low Phase Noise Applications

Features

- Frequency range
  - 5 GHz in 10/11 prescaler modulus
  - 4 GHz in 5/6 prescaler modulus
- Phase noise floor figure of merit:
  - –225 dBc/Hz
- Selectable prescaler modulus of 5/6 or 10/11
- Low power
  - 80 mA @ 2.8V
- Serial or direct mode access
- Internal phase detector
- Frequency selectivity
  - comparison frequency/2^{18}

100 krad (Si) total dose

Product Description

The PE97640 is a radiation tolerant, high performance, fractional-N PLL capable of frequency synthesis up to 5 GHz. The device is optimized for commercial space applications and superior phase noise performance.

The PE97640 features a 5/6 or 10/11 dual modulus prescaler, counters, a delta sigma modulator, a phase comparator and charge pump as shown in *Figure 1*. Counter values are programmable through either a serial interface or directly hard-wired.

The PE97640 is available in a 64-lead CQFP and is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Figure 1. Functional Diagram

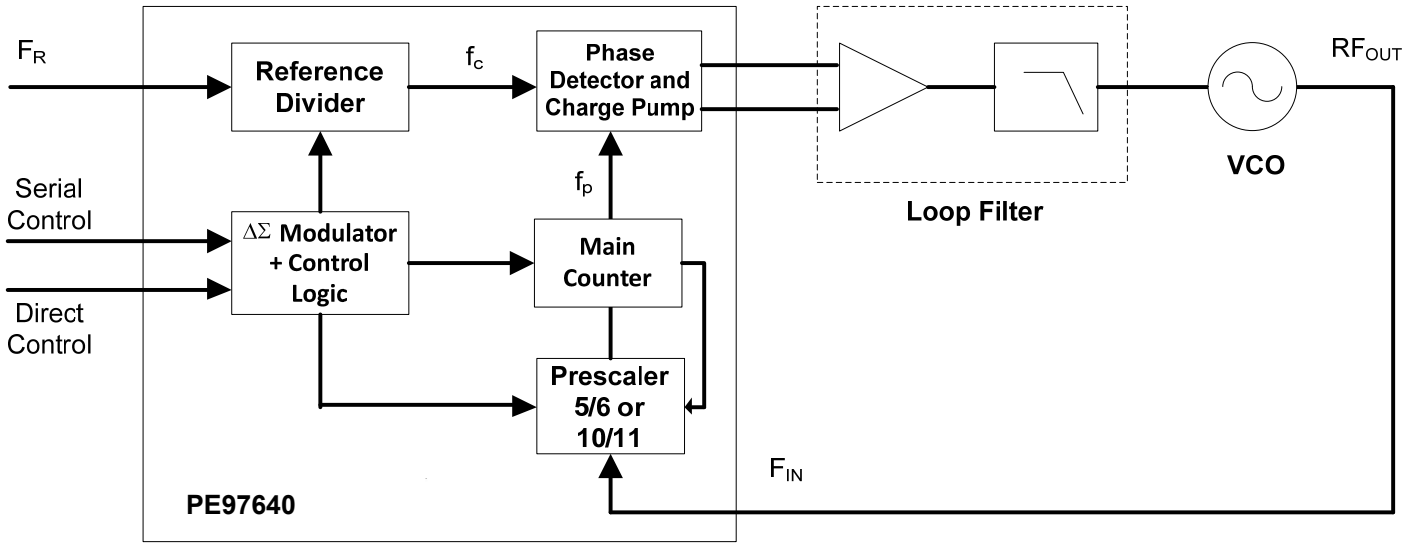


Figure 2. Pin Configuration (Top View)

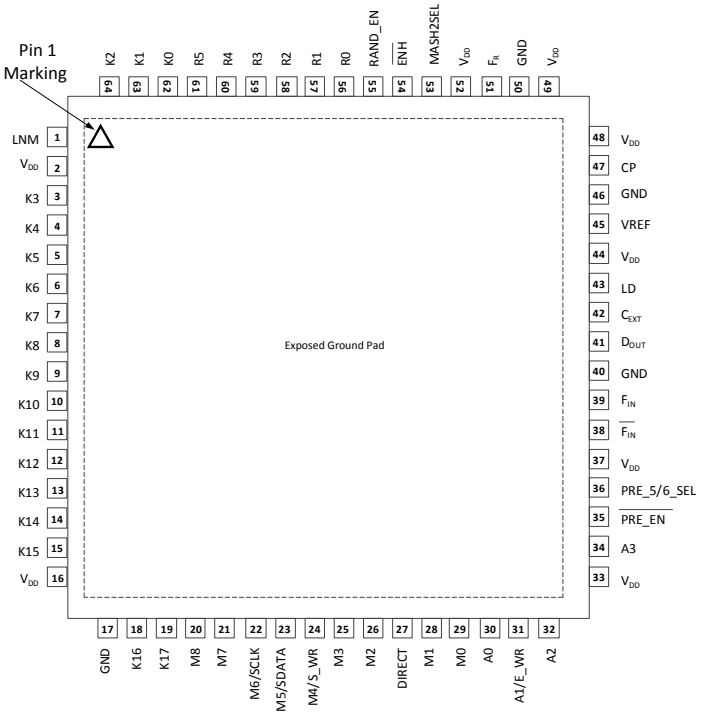


Figure 3. Package Type

64-lead CQFP

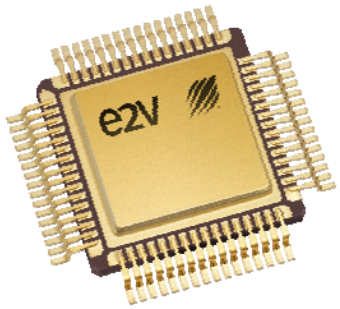


Table 1. Pin Descriptions

Pin #	Pin Name	Valid Mode	Type	Description
1	LNM	Both	Note 2	Low noise mode. “High” selects low noise mode. “Low” selects normal mode.
2	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
3	K3	Direct	Note 2	K counter bit3
4	K4	Direct	Note 2	K counter bit4
5	K5	Direct	Note 2	K counter bit5
6	K6	Direct	Note 2	K counter bit6
7	K7	Direct	Note 2	K counter bit7
8	K8	Direct	Note 2	K counter bit8
9	K9	Direct	Note 2	K counter bit9
10	K10	Direct	Note 2	K counter bit10
11	K11	Direct	Note 2	K counter bit11

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
12	K12	Direct	Note 2	K counter bit12
13	K13	Direct	Note 2	K counter bit13
14	K14	Direct	Note 2	K counter bit14
15	K15	Direct	Note 2	K counter bit15
16	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
17	GND	Both		Ground
18	K16	Direct	Note 2	K counter bit16
19	K17	Direct	Note 2	K counter bit17
20	M8	Direct	Note 2	M counter bit8 (MSB)
21	M7	Direct	Note 2	M counter bit7
22	SCLK	Serial	Note 2	Serial clock input. SDATA is clocked serially into the 21-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
	M6	Direct	Note 2	M counter bit6
23	SDATA	Serial	Note 2	Binary serial data input. Input data entered MSB first.
	M5	Direct	Note 2	M counter bit5
24	S_WR	Serial	Note 2	Serial load enable input. While S_WR is “low”, SDATA can be serially clocked. Primary register data is transferred to the secondary register on S_WR rising edge.
	M4	Direct	Note 2	M counter bit4
25	M3	Direct	Note 2	M counter bit3
26	M2	Direct	Note 2	M counter bit2
27	DIRECT	Both	Note 2	Direct mode select. “High” enables direct mode. “Low” enables serial mode.
28	M1	Direct	Note 2	M counter bit1
29	M0	Direct	Note 2	M counter bit0 (LSB)
30	A0	Direct	Note 2	A counter bit0 (LSB)
31	E_WR	Serial	Note 2	Enhancement register write enable. While E_WR is “high”, SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
	A1	Direct	Note 2	A counter bit1
32	A2	Direct	Note 2	A counter bit2
33	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
34	A3	Direct	Note 2	A counter bit3
35	$\overline{\text{PRE\_EN}}$	Direct	Note 2	Prescaler enable, active “low”. When “high”, F_{IN} bypasses the prescaler.
36	PRE_5/6_SEL	Direct	Note 2	5/6 modulus select, active “High.” When “Low,” 10/11 modulus selected.
37	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
38	$\overline{F_{IN}}$	Both	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground.

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
39	F_{IN}	Both	Input	Prescaler input from the VCO. A 22 pF coupling capacitor should be placed as close as possible to this pin and be connected in shunt to a 50Ω resistor to ground.
40	GND	Both		Ground
41	D_{OUT}	Both	Output	Data out function, enabled in enhancement mode.
42	C_{EXT}	Both	Output	Logical "NAND" of internal PFD outputs, PD_$\overline{D}$ and PD_$\overline{U}$, through an on chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
43	LD	Both	Output	Lock detect and open drain logical inversion of C_{EXT}. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0").
44	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
45	VREF	Both	Output	Charge pump reference voltage
46	GND	Both		Ground
47	CP	Both	Output	Charge pump output
48	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
49	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
50	GND	Both		Ground
51	F_R	Both	Input	Reference frequency input
52	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
53	MASH2SEL	Both	Note 2	MASH 1-1 select. "High" selects MASH 1-1 mode. "Low" selects the MASH 1-1-1 mode.
54	$\overline{ENH}$	Both	Note 2	Enhancement mode. When asserted low ("0"), enhancement register bits are functional.
55	RAND_EN	Both	Note 2	K register LSB toggle enable. "1" enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the phase detector comparison frequency/2^{19}.
56	R0	Direct	Note 2	R counter bit0 (LSB)
57	R1	Direct	Note 2	R counter bit1
58	R2	Direct	Note 2	R counter bit2
59	R3	Direct	Note 2	R counter bit3
60	R4	Direct	Note 2	R counter bit4
61	R5	Direct	Note 2	R counter bit5 (MSB)
62	K0	Direct	Note 2	K counter bit0 (LSB)
63	K1	Direct	Note 2	K counter bit1
64	K2	Direct	Note 2	K counter bit3
Pad	GND			Exposed pad: grounded for proper operation.

Notes: 1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-down resistors to ground.

Table 2. Operating Ranges

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	2.6	2.8	V
Operating ambient temperature range	T_A	–40	+85	°C

Table 3. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	3.3	V
Voltage on any input	V_I	–0.3	V_{DD} + 0.3	V
DC into any input	I_I	–10	+10	mA
DC into any output	I_O	–10	+10	mA
Theta JC	θ_{JC}		23	°C/W
Junction temperature maximum	T_j		+125	°C
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM*	V_{ESD_HBM}		500	V
RF input power, CW 50 MHz-5 GHz	P_{MAX-CW}		10	dBm

Note: * Human Body Model (MIL-STD 883 Method 3015).

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements and therefore do not exhibit enhanced low dose rate sensitivity.

Table 4. DC Characteristics @ V_{DD} = 2.7V, –40 °C < T_A < 85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Operational supply current	Prescaler disabled, f_c = 50 MHz, F_{IN} = 500 MHz		41		mA
		5/6 prescaler, f_c = 50 MHz, F_{IN} = 3 GHz		80		mA
		10/11 prescaler, f_c = 50 MHz, F_{IN} = 3 GHz		82		mA
All digital inputs: K[17:0], R[5:0], M[8:0], A[3:0], Direct, $\overline{\text{PRE\_EN}}$, RAND_EN, MASH2_SEL, $\overline{\text{ENH}}$, LMN (have a 70 kΩ pull-down resistor)						
V_{IH}	High level input voltage		0.7 x V_{DD}			V
V_{IL}	Low level input voltage				0.3 × V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 2.7V			100	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} 2.7V	–10			µA
Reference divider input: F_R						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 2.7V			300	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 2.7V	–300			µA
Charge Pump and VREF outputs: CP, VREF						
I_{CPH}	Charge pump output current	V_{CP} = V_{DD} / 2		2.5		mA
I_{CPL}	Charge pump output current	V_{CP} = V_{DD} / 2		–2.5		mA
VREF	Charge pump reference voltage	V_{DD} = 2.7V		1.35		V

Table 4. DC Characteristics (cont.) @ V_{DD} = 2.7V, –40 °C < T_A < 85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital test outputs: D_{OUT} (totem-pole)						
V_{OLD}	Output voltage LOW	I_{OUT} = 200 µA			0.4	V
V_{OHD}	Output voltage HIGH	I_{OUT} = –200 µA	V_{DD} – 0.4			V
Lock detect outputs: (C_{EXT} <totem-pole>**, LD** <open-drain CMOS>**)**						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{OUT} = 0.1 mA			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{OUT} = –0.1 mA	V_{DD} – 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{OUT} = 1 mA			0.4	V

Table 5. AC Characteristics @ V_{DD} = 2.7V, –40 °C < T_A < 85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see *Figures 7* and *8*)						
f_{Clk}	Serial data clock frequency[1]				10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	SDATA set-up time to SCLK rising edge		10			ns
t_{DHLD}	SDATA hold time after SCLK rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	SCLK rising edge to S_WR rising edge		30			ns
t_{CE}	SCLK falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to SCLK rising edge		30			ns
t_{EC}	E_WR transition to SCLK rising edge		30			ns
Main divider 10/11 (including prescaler)						
P_{F_IN}	Input level range	External AC coupling 4 GHz ≤ freq ≤ 5 GHz	–3[2]		5	dBm
Main divider 5/6 (including prescaler)						
P_{F_IN}	Input level range	External AC coupling 800 MHz ≤ freq < 4 GHz	–3[2]		5	dBm
Main divider (prescaler bypassed)						
F_{IN}	Operating frequency		50		800	MHz
P_{F_IN}	Input level range	External AC coupling	–5[2]		5	dBm
Reference divider						
F_R	Operating frequency				100	MHz
P_{FR}	Reference input power[3]	Single-ended input	–5[4]		7	dBm
Phase detector						
f_c	Comparison frequency				50	MHz

Table 5. AC Characteristics @ V_{DD} = 2.7V, –40 °C < T_A < 85 °C, unless otherwise specified (cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SSB phase noise 5/6 prescaler (F_{IN} = 3 GHz, f_c = 50 MHz, LBW = 150 kHz, LNM mode)						
Φ_N	Phase noise	100 Hz offset		–95		dBc/Hz
Φ_N	Phase noise	1 kHz offset		–102		dBc/Hz
Φ_N	Phase noise	10 kHz offset		–110		dBc/Hz
Φ_N	Phase noise	50 kHz offset		–112		dBc/Hz
SSB phase noise 10/11 prescaler (F_{IN} = 4 GHz, f_c = 25 MHz, LBW = 150 kHz)						
Φ_N	Phase noise	100 Hz offset		–92		dBc/Hz
Φ_N	Phase noise	1 kHz offset		–99		dBc/Hz
Φ_N	Phase noise	10 kHz offset		–105		dBc/Hz
Φ_N	Phase noise	50 kHz offset		–105		dBc/Hz
Phase noise figure of merit (FOM)[5]						
$FOM_{flicker}$	Flicker figure of merit	5/6 prescaler		–263		dBc/Hz
		10/11 prescaler		–260		dBc/Hz
FOM_{floor}	Floor figure of merit	5/6 prescaler		–225		dBc/Hz
		10/11 prescaler		–223		dBc/Hz
$FOM_{flicker}$	$PN_{flicker} = FOM_{flicker} + 20\log(f_{vco}) - 10\log(f_{offset})$					dBc/Hz
FOM_{floor}	$PN_{floor} = FOM_{floor} + 10\log(f_{pfd}) + 20\log(f_{vco}/f_{pfd})$					dBc/Hz
FOM_{total}	$PN_{total} = 10\log(10\,[PN_{flicker}/10] + 10\,[PN_{floor}/10])$					dBc/Hz

Notes: 1. f_{clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk} specification.
2. 0 dBm minimum is recommended for improved phase noise performance when sine-wave is applied.
3. CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of the PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled. For sine-wave inputs, the minimum amplitude needs to be 0.5 V_{PP}. The maximum level should be limited to prevent ESD diodes at the pin input from turning on. Diodes will turn on at one forward-bias diode drop above V_{DD} or below GND. The DC voltage at the Reference input is $V_{DD}/2$.
4. +2 dBm or higher is recommended for improved phase noise performance.
5. The phase noise can be separated into two normalized specifications: a floor figure of merit and a flicker figure of merit. To accurately measure the phase noise floor without the contribution of the flicker noise, the loop bandwidth is set to 150 kHz and the phase noise is measured at a frequency offset near 50 kHz. The flicker noise is measured at a frequency offset ≤ 1000 Hz. The formula assumes a –10 dB/decade slope versus frequency offset.

Figure 4. Equivalent Input Diagram: Digital Input

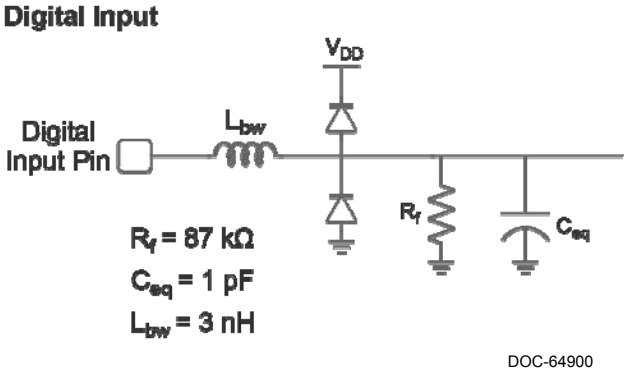


Figure 5. Equivalent Input Diagram: Reference Input

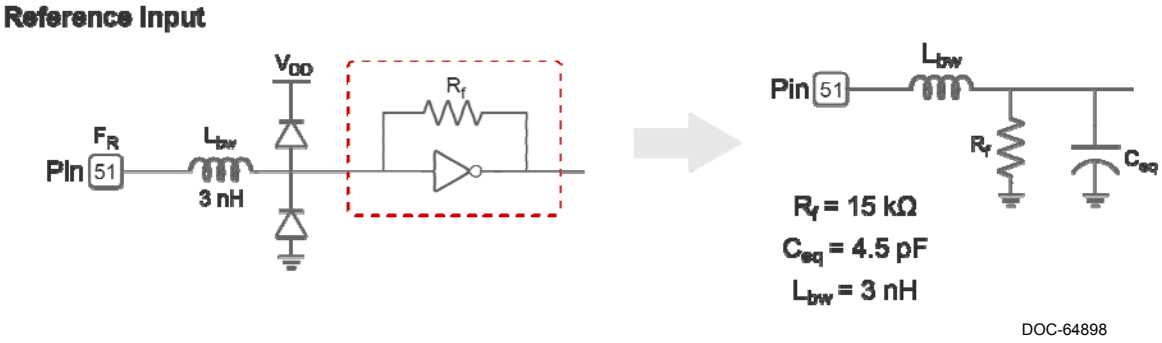
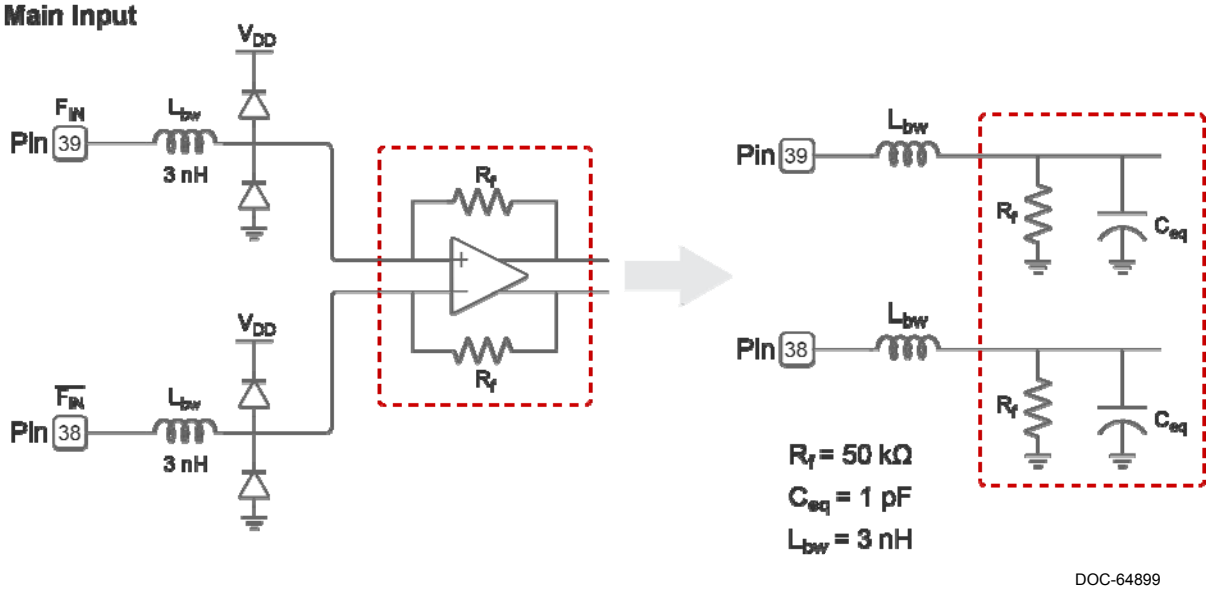


Figure 6: Equivalent Input Diagram: Main Input

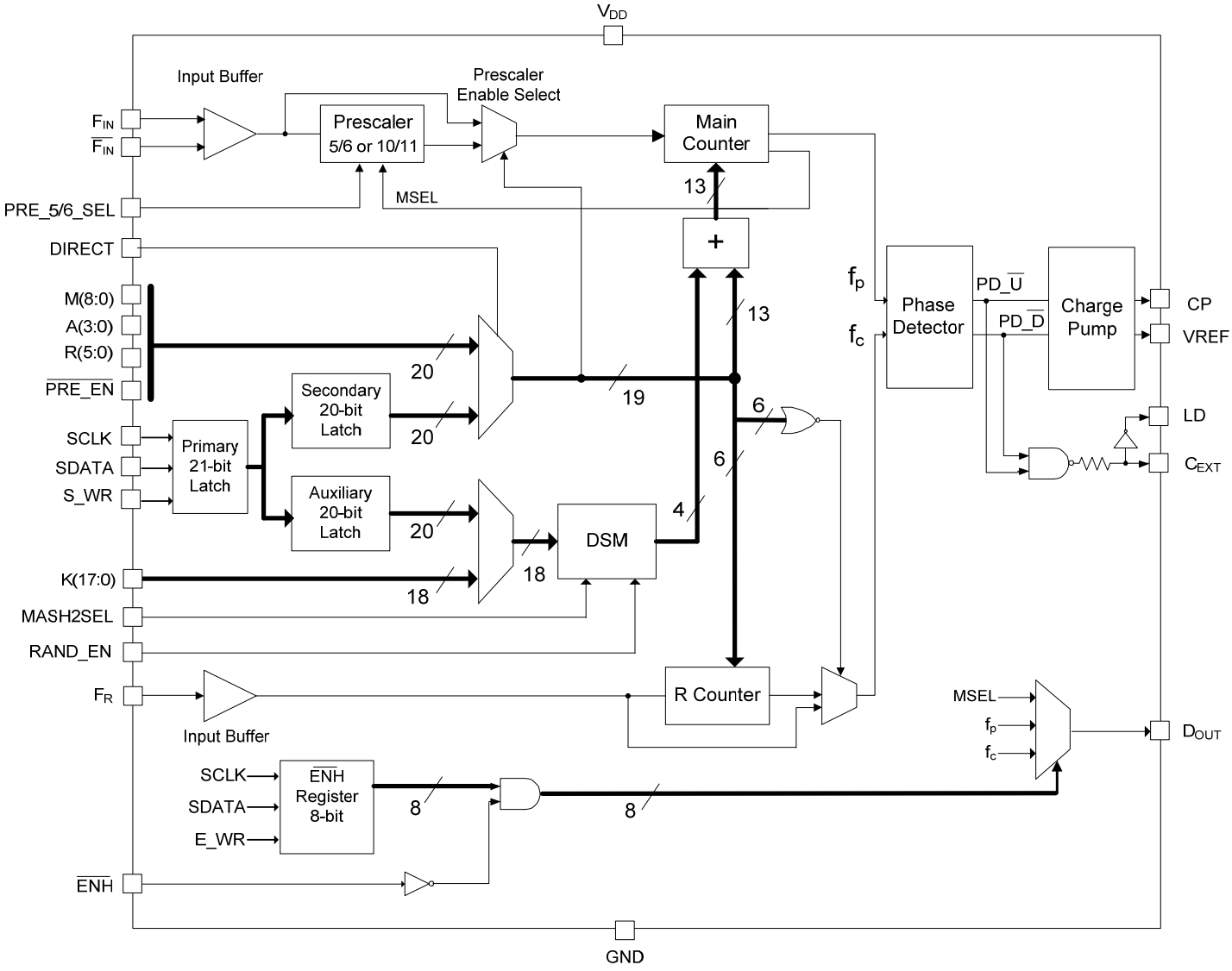


Functional Description

The PE97640 consists of a prescaler, counters, an 18-bit delta-sigma modulator (DSM), a phase detector and charge pump. The dual modulus prescaler divides the VCO frequency by either 5/6 or 10/11, depending on the value of the modulus select. Counters R and M divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (A) is used in the modulus select logic. The DSM modulates the A counter outputs in order to achieve the desired fractional step.

The phase detector generates up and down frequency control signals that drive the charge pump. Data is written into the internal registers via the three wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 7. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

Setting the $\overline{\text{PRE\_EN}}$ control bit LOW enables the ÷ 5/6 or ÷ 10/11 prescaler. The prescaler can be set to either a 5/6 or 10/11 modulus based on the PRE_5/6_SEL pin. The main counter chain divides the RF input frequency (F_{IN}) by an integer or fractional number derived from the values in the M, A counters and the DSM input word K.

The part can be operated in Integer-N mode or in two different fractional-n modes. Setting K = 0 operates the part in integer-n mode. Setting K to a non-zero value operates the part in either fractional-n mode. The fractional-n modes use a MASH (**M**ulti-st**A**ge noise **SH**aping) decimation structure.

The MASH-1-1 mode is a 2nd order fractional dithering using four (2^2) N values: N-1, N, N+1, N+2.

MASH-1-1-1 mode is a 3rd order fractional dithering using eight (2^3) N values: N-3, N-2, N-1, N, N+1, N+2, N+3, N+4.

Setting the MASH2SEL pin HIGH enables MASH-1-1 mode and LOW enables MASH-1-1-1 mode. MASH-1-1 has a 40 dB/dec slope away from the carrier while MASH-1-1-1 has a 60 dB/dec slope.

The 18-bit accumulator size fixes the fractional value to $K/2^{18}$. However, there is an additional bit in the DSM that acts like an extra bit (19^{th} bit). This bit is enabled by setting the RAND_EN pin HIGH. Enabling this bit has the benefit of reducing the spurious levels. However, a small, positive frequency offset will occur which is calculated as

$$F_{offset} = [F_R / (R + 1)] / 2^{19} \quad (1)$$

Using the part in either MASH mode will yield a fractional spur at

$$F_{spur} =$$

$$[(2K + RAND\_EN) / 2^{19}] \times f_c \quad 1 \leq K \leq 2^{17} \quad (2)$$

$$[1 - (2K + RAND\_EN) / 2^{19}] \times f_c \quad (2^{17} + 1) \leq K \leq (2^{18} - 1)$$

Where f_c is the comparison frequency.

MASH-1-1-1 mode reduces this spur for an increase in the phase noise and decrease in the number of valid programming frequencies.

All of the following equations do not take into account the frequency offset from RAND_EN. If this offset is important to a specific frequency plan, it should be taken into account accordingly.

During normal operation, the output from the main counter chain (f_p) is related to the VCO frequency (F_{IN}) by the following equations:

10/11 modulus

$$f_p = F_{IN} / (N + K / 2^{18}) \quad (3)$$

where

$$N = 10 \times (M + 1) + A$$

$$A \leq M + 1,\ 1 \leq M \leq 511$$

5/6 modulus

$$f_p = F_{IN} / [N + K / 2^{18}] \quad (4)$$

where

$$N = 5 \times (M + 1) + A$$

$$A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

10/11 modulus

$$F_{IN} = [N + K / 2^{18}] \times [F_R / (R + 1)] \quad (5)$$

where

$$N = 10 \times (M + 1) + A$$

$$A \leq M + 1,\ 1 \leq M \leq 511$$

5/6 modulus

$$F_{IN} = (N + K / 2^{18}) \times [F_R / (R + 1)] \quad (6)$$

where

$$N = 5 \times (M + 1) + A$$

$$A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that:
In Integer-N mode, to obtain contiguous channels,

F_{IN} must be ≥ 90 x [F_R / (R + 1)] with 10/11 modulus.

F_{IN} must be ≥ 20 x [F_R / (R + 1)] with the 5/6 modulus.

In MASH-1-1 mode, to obtain contiguous channels,

F_{IN} must be ≥ 91 x [F_R / (R + 1)] with 10/11 modulus.

F_{IN} must be ≥ 21 x [F_R / (R + 1)] with 5/6 modulus.

In MASH-1-1-1 mode, to obtain contiguous channels,

F_{IN} must be ≥ 93 x [F_R / (R + 1)] with 10/11 modulus.

F_{IN} must be ≥ 23 x [F_R / (R + 1)] with 5/6 modulus.

The A counter can accept values as high as 15, but in typical operation it will cycle from 0-to-9 between increments in M. Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode

Setting the frequency control register bit $\overline{\text{PRE\_EN}}$ HIGH allows F_{IN} to bypass the ÷ 5/6 or ÷ 10/11 prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly.

The following equation relates F_{IN} to the reference frequency F_R:

$$F_{IN} = (M + 1 + K / 2^{18}) \times [F_R / (R + 1)] \quad (7)$$

where

Int-N mode	$1 \le M \le 511$
MASH-1-1 mode	$2 \le M \le 509$
MASH-1-1-1 mode	$4 \le M \le 507$

Reference Counter

The reference counter chain divides the reference frequency F_R down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \quad (8)$$

where

$0 \le R \le 63$

Note that programming R with “0” will pass the reference frequency (F_R) directly to the phase detector.

Serial Interface Mode

While the E_WR input is LOW and the S_WR input is LOW, serial input data (SDATA input), B_0 to B_{20}, is clocked serially into the primary register on the rising edge of SCLK, MSB (B_0) first. The contents from the primary register are transferred into either the secondary register or the auxiliary register on the rising edge of S_WR depending on the value of the address bit (B20) according to the timing diagram shown in *Figure 8*. Data is transferred to the counters as shown in *Table 7* and *Table 8.*

While the E_WR input is HIGH and the S_WR input is LOW, serial input data (SDATA input), B_0 to B_7, is clocked serially into the enhancement register on the rising edge of SCLK, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in *Figure 8*. After the falling edge of E_WR, the data provides control bits as shown in *Table 9* and *Table 10* with bit functionality enabled by asserting the $\overline{\text{ENH}}$ input LOW.

Direct Interface Mode

Direct Interface Mode is selected by setting the Direct input HIGH.

Counter control bits are set directly at the pins as shown in *Table 7* and *Table 8*. The counters will load from the pin states upon terminal count.

Phase Detector

The phase detector is triggered by rising edges from the main counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_$\overline{\text{D}}$ and PD_$\overline{\text{U}}$. These outputs are internal signals and are not brought out to pins. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_$\overline{\text{D}}$ pulses LOW. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), PD_$\overline{\text{U}}$ pulses LOW. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

A lock detect output, LD is also provided, via the pin C_{EXT}. C_{EXT} is the logical NAND of PD_$\overline{\text{U}}$ and PD_$\overline{\text{D}}$ waveforms, which is driven through a series 2 kΩ resistor. Connecting C_{EXT} to an external shunt capacitor provides low pass filtering of this signal. C_{EXT} also drives the input of an internal inverting comparator with an open drain output. Thus LD is an AND function of PD_$\overline{\text{U}}$ and PD_$\overline{\text{D}}$.

Charge Pump

The charge pump is driven by the two outputs from the phase detector. If the divided VCO leads the divided reference in phase or frequency (f_p lead f_c), the charge pump will source current from V_{DD}. The charge pump source and sink current varies proportionally with the voltage at the CP pin. These two currents have a matching value near 2.5 mA at a V_{CP} of $V_{DD}/2$. The VREF pin provides a reference voltage of $V_{DD}/2$. It is necessary to use the charge pump with an active loop filter as shown in *Figure 1*.

An external resistor is required from the charge pump output to V_{DD}. This resistor enhances the phase noise performance by improving the linearity of the charge pump.

Low Noise Mode

During normal operation, the charge pump can generate digital noise, which can result in slightly higher phase noise. Low noise mode can be used to keep noisy digital events consistently the same at critical moments when charge pump is on. The following conditions apply to the programming of the M and A counters for each mode of operation.

5/6 Prescaler

Sometimes simply using A > 4 alone without activating LNM mode can achieve similar phase noise improvement as LNM mode. In these cases, using normal mode is preferred because the limitation of equation (10) under LNM mode will not apply. What will apply for A > 4 becomes M ≥ A–2 or equivalently, A ≤ M+2, which is less restrictive.

For 5/6 prescaler mode, the M and A counters in normal mode are equivalent to M-1 and A+5 in LNM mode. In normal mode, A=0-to-4 are typically used, which has only five A codes needed to fully program contiguous frequencies. In LNM mode, A=3-to-7 or A=4-to-8 can be used, which still guarantees five A codes to provide fully contiguous frequencies.

5/6 Modulus LNM

$$\boldsymbol{3 \le A \le 11} \qquad \textbf{(9)}$$

$$\boldsymbol{M \ge A+3 \text{ or equivalently, } A \le M-3} \qquad \textbf{(10)}$$

10/11 Prescaler

In 10/11 prescaler mode, the M and A counters in normal mode are equivalent to M–1 and A+10 in LNM mode. In normal mode, A=0-to-9 are typically used and in most cases, A=0, 1, 2, 7, 8 and 9 may exhibit slightly higher phase noise compared to LNM mode. In these cases, a user should program both M and A=0-to-M-1 and A=10, and M and A=1-to-M-1 and A=11. For example:

Table 6. M and A Counters

Normal Mode		Low Noise Mode	
M	A	M	A
15	0	14	10
15	1	14	11

For all other A values except for A=2, simply enable LNM mode if the phase noise improvement in LNM mode is significant compared to normal mode. The following equations define the programming range limitations for the LNM mode. For A=2, it can only be operated in normal mode.

10/11 Modulus LNM

$$\boldsymbol{3 \le A \le 11} \qquad \textbf{(11)}$$

$$\boldsymbol{M \ge A+3 \text{ or equivalently, } A \le M-3} \qquad \textbf{(12)}$$

Table 7. Secondary Register Programming

Interface Mode	$\overline{ENH}$	R_5	R_4	M_8	M_7	$\overline{PRE\_EN}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	Addr
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	B_{20}
Direct	1	R_5	R_4	M_8	M_7	$\overline{PRE\_EN}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	0

Note: * Serial data clocked serially on SCLK rising edge while E_WR LOW and captured in secondary register on S_WR rising edge.

MSB (first in) (last in) LSB

Table 8. Auxiliary Register Programming

Interface Mode	$\overline{ENH}$	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	Rsrv	Rsrv	Addr
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	B_{20}
Direct	1	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	X	X	1

Note: * Serial data clocked serially on SCLK rising edge while E_WR LOW and captured in auxiliary register on S_WR rising edge.

MSB (first in) (last in) LSB

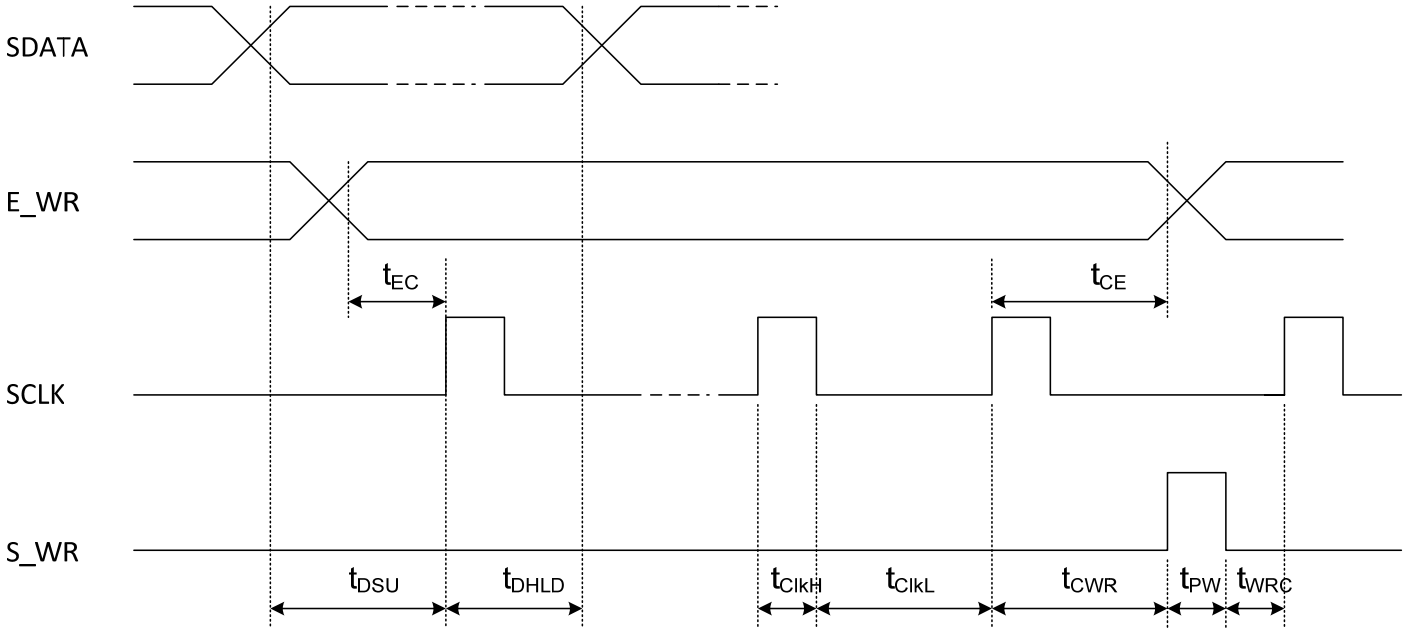
Table 9. Enhancement Register Programming

Interface Mode	$\overline{ENH}$	Direct	Reserved	Reserved	f_p output	Power Down	Counter load	MSEL output	f_c output	LD Disable
Serial*	0	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

Note: * Serial data clocked serially on SCLK rising edge while E_WR HIGH and captured in the double buffer on E_WR falling edge.

MSB (first in) (last in) LSB

Figure 8. Serial Interface Mode Timing Diagram



Enhancement Register

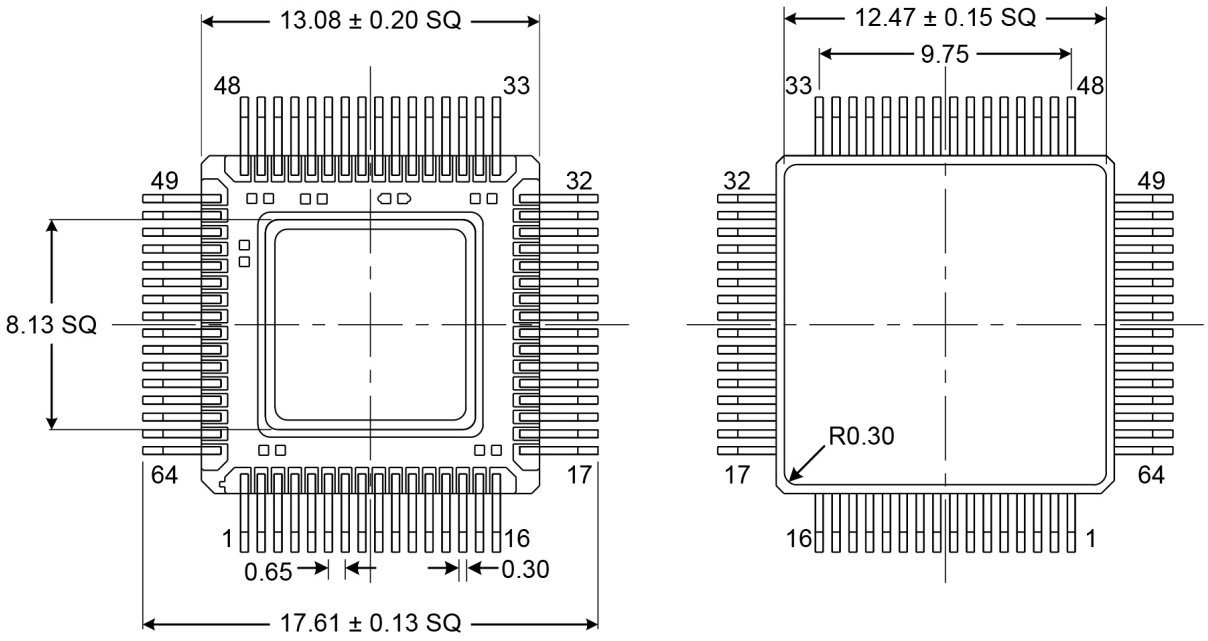
The functions of the enhancement register bits are shown below with all bits active “high”.

Table 10. Enhancement Register Bit Functionality

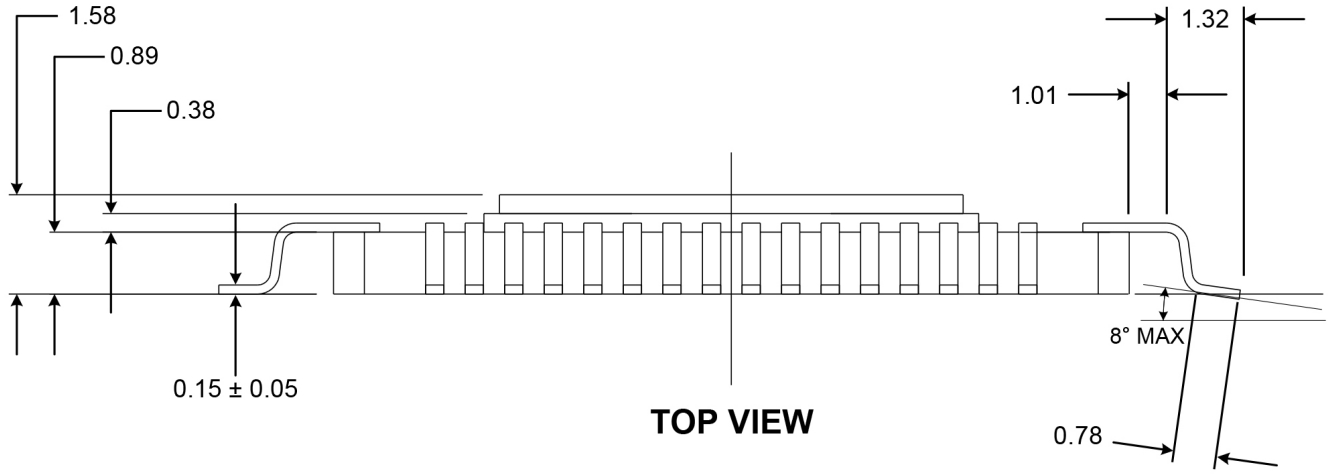
Bit Function		Description
Bit 0	Reserve*	Reserved.
Bit 1	Reserve*	Reserved.
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the reference counter output onto the D_{OUT} output.
Bit 7	LD disable	Disables the LD pin for quieter operation.

Note: * Program to 0.

Figure 9. Package Drawing (dimensions are in millimeters)
64-lead CQFP



TOP VIEW **BOTTOM VIEW**



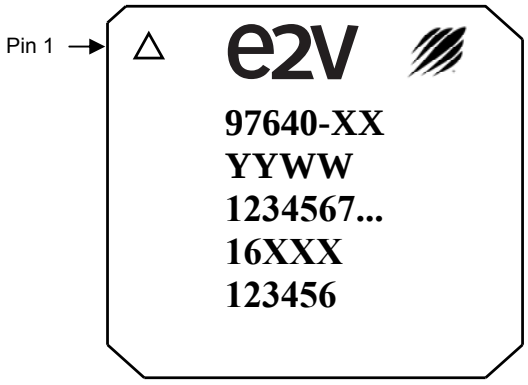
TOP VIEW

LEADTIPS 0.10 MM COPLANARITY
AND PLANAR WITH
BOTTOM OF EXPOSED GROUND
PAD WITHIN 0.20 MM

DIMS IN MM.
ALL TOLERANCES ARE +/- 0.127
UNLESS OTHERWISE STATED.
NOT TO SCALE

REV 99, 102017

Figure 10. Top Marking Specifications



Not to scale PRT-55218

Line 1: Pin 1 indicator △, e2v and Peregrine logo
Line 2: Part number (XX will be specified by the purchase order)
Line 3: Date code (last two digits of the year and work week)
Line 4: Wafer lot # (as many characters as room allows)
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside marking on any of the Peregrine products.

Table 11. Ordering Information

Order Code	Description	Packaging	Shipping Method
97640-01*	Engineering samples	64-lead CQFP	Tray
97640-11	Flight units	64-lead CQFP	Tray
97640-00	Evaluation kit		1/Box

Note: * The 97640-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE97640-11 flight units. The PE97640-01 device provides the same functionality and footprint as the PE97640-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
Teledyne e2v Hirel Electronics ~ www.tdehirel.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).