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Peregrine Semiconductor

Product Specification

PE9354

SPDT High Power UltraCMOS® RF Switch Radiation Tolerant for Space Applications

Features

- Single +3V power supply
- Low insertion loss: 0.55 dB @ 2000 MHz
- High isolation of 30 dB @ 2000 MHz
- Typical input P1dB compression point of +31 dBm
- 100 krad(Si) total dose
- Single-pin CMOS or TTL logic control

Product Description

The PE9354 SPDT high power UltraCMOS® RF switch is designed to cover a broad range of applications from near DC to 3000 MHz. This single-supply reflective switch integrates on-board CMOS control logic driven by a simple, single-pin CMOS and TTL compatible control input. Using a nominal +3V power supply, a typical input P1dB compression point of +31 dBm can be achieved. The PE9354 also exhibits input-output isolation of better than 30 dB at 2000 MHz and is offered in a small 8-lead CFP.

The PE9354 is optimized for commercial space applications and is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance. Single event latch-up (SEL) is physically impossible and single event upset (SEU) is better than 10^{-9} errors per bit/day.

Figure 2. Package Type
8-lead CFP

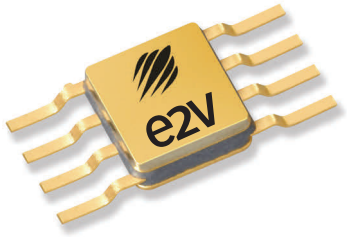


Figure 1. Functional Diagram

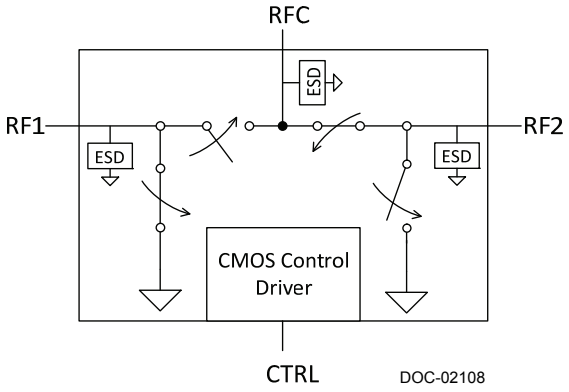


Table 1. AC Electrical Specifications @ –40 °C to +85 °C, V_{DD} = 3.0V (Z_S = Z_L = 50Ω)[1]

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency[2]		DC		3000	MHz
Insertion loss	2000 MHz		0.55	0.80	dB
Isolation – RFC to RF1/RF2	2000 MHz	28	32		dB
Isolation – RF1 to RF2	2000 MHz	24	28		dB
Return loss[3]	2000 MHz		22		dB
Input P1dB compression point	2000 MHz	28	31		dBm

Notes: 1. Parameters are tested in production at –40 °C and +85 °C.
2. Device linearity will begin to degrade below 10 MHz.
3. Return loss not measured in production due to equipment limitations.

Figure 3. Pin Configuration

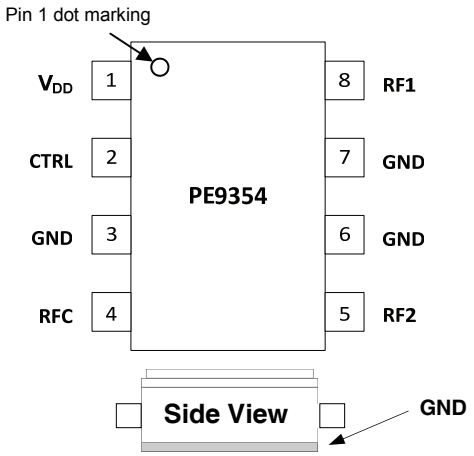


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	V_{DD}	Nominal +3V supply connection.
2	CTRL	CMOS or TTL logic level: High = RFC to RF1 signal path. Low = RFC to RF2 signal path.
3	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
4	RFC	Common RF port for switch.*
5	RF2	RF2 port.*
6	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
7	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
8	RF1	RF1 port.*
GND	GND	Bottom of the package is ground. Connecting the bottom of the package to ground is required

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. DC Electrical Specifications

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.7	3.0	3.3	V
Input leakage	–1		1	µA
Supply current, I_{DD} (V_{DD} = 3V, V_{CTRL} = 3V)		28	100	µA
Control voltage high	0.7 × V_{DD}			V
Control voltage low			0.3 × V_{DD}	V

Absolute maximum ratings are those values listed in the following table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	–0.3	4.0	V
V_I	Voltage on any input except for the CTRL input	–0.3	V_{DD} + 0.3	V
V_{CTRL}	Voltage on CTRL input		5.0	V
T_{ST}	Storage temperature range	–65	+150	°C
T_{OP}	Operating temperature range	–40	+85	°C
P_{IN}	Input power (50Ω)		32	dBm
Θ_{JC}	Theta JC		57	°C/W
T_j	Junction temperature		+125	°C
V_{ESD}	ESD voltage (Human Body Model)		200	V
TID	Total cumulative exposure to ionizing radiation		100	kRad(Si)

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 3*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFC to RF1
CTRL = CMOS or TTL Low	RFC to RF2

The control logic input pin (CTRL) is typically driven by a +3V CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Typical Performance Data @ V_{DD} = 3V

Figure 4. Insertion Loss – RFC to RF1

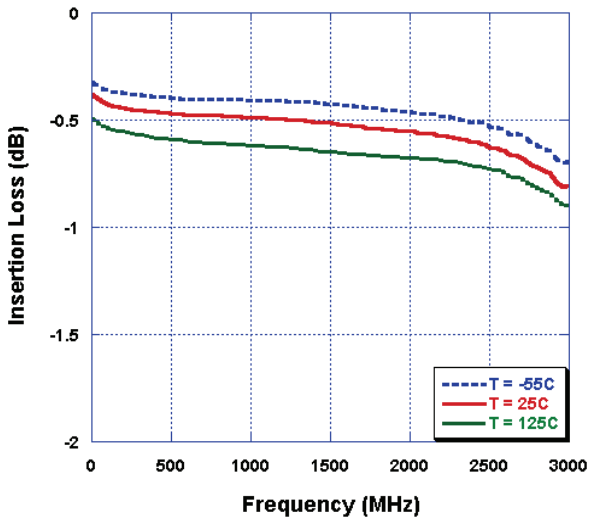


Figure 5. Input P1dB Compression Point

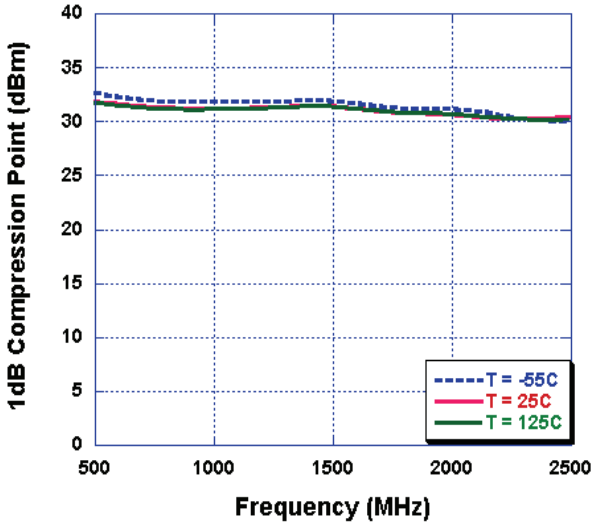


Figure 6. Insertion Loss – RFC to RF2

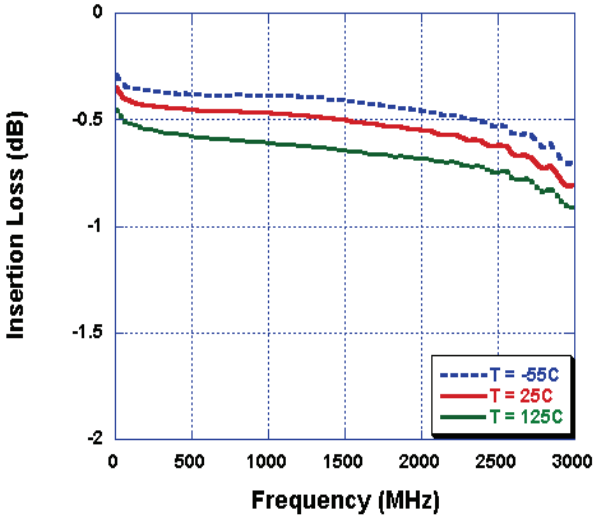
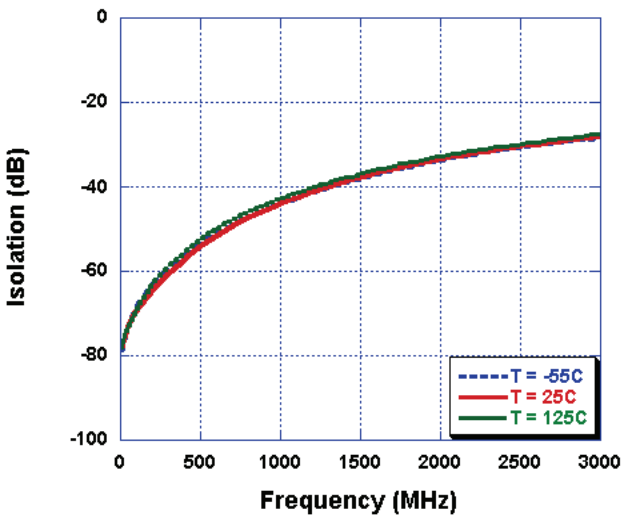


Figure 7. Isolation – RFC to RF1



Typical Performance Data @ V_{DD} = 3V (cont.)

Figure 8. Isolation – RFC to RF2

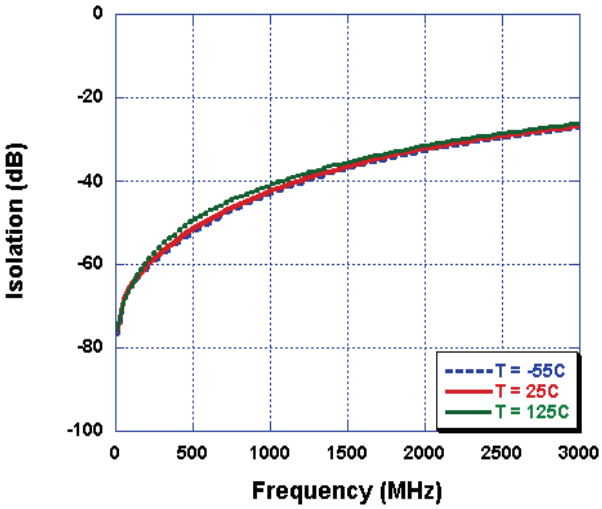


Figure 9. Isolation – RF1/RF2 to RF2/RF1

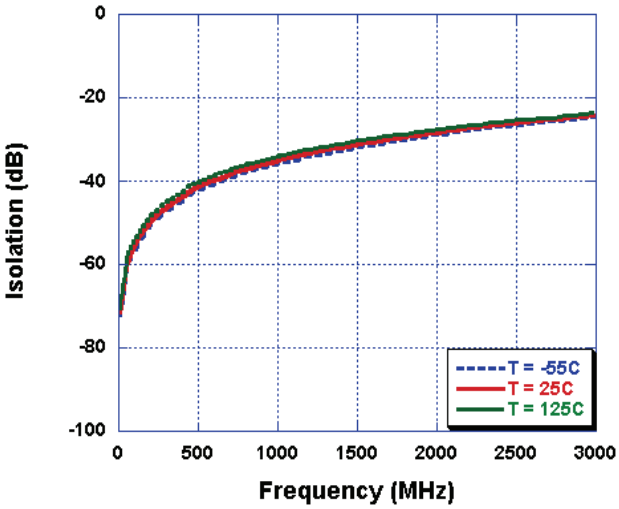


Figure 10. Return Loss – RFC

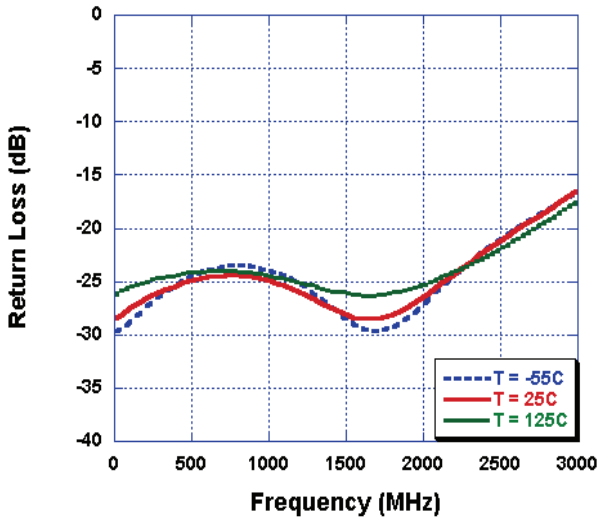


Figure 11. Return Loss – RF1, RF2

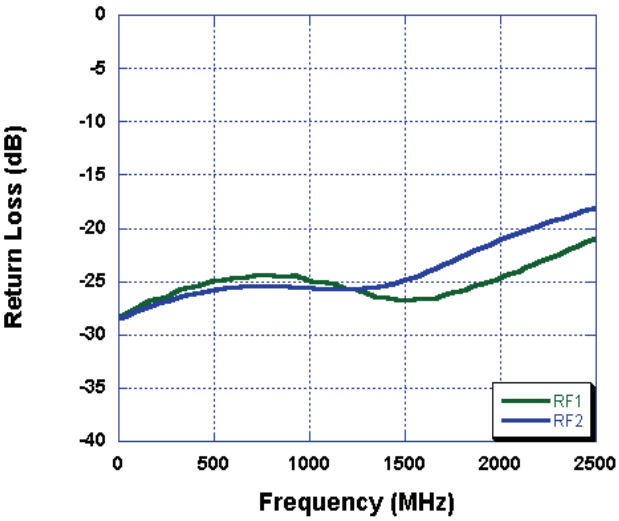
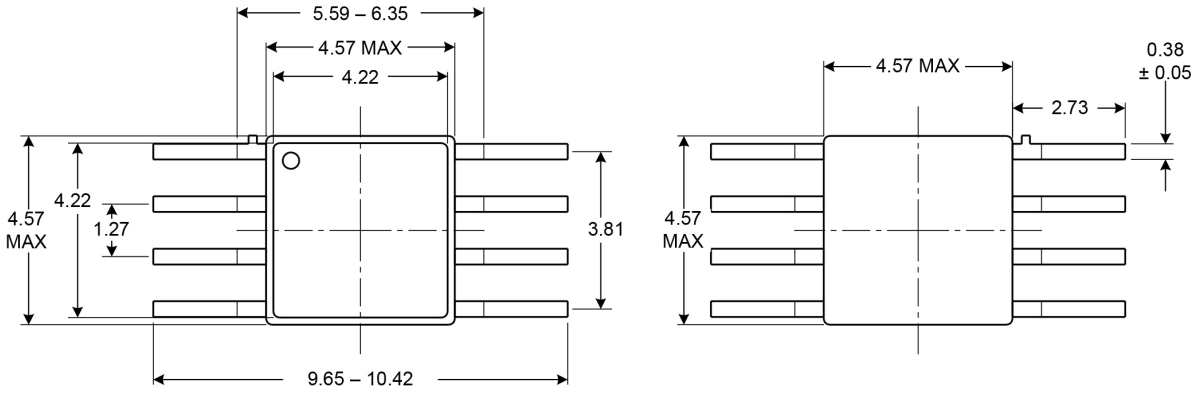


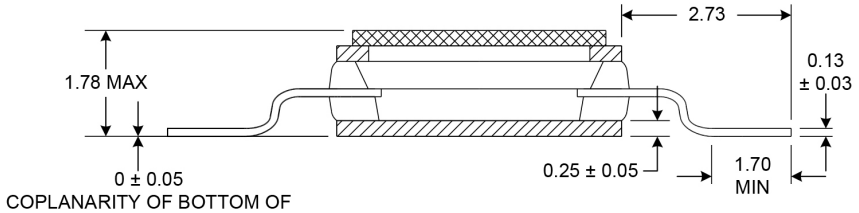
Figure 14. Package Drawing (dimensions are in millimeters)

8-lead CFP

Note: Bottom of the package is ground. Connecting the bottom of the package to ground is required.



TOP VIEW **BOTTOM VIEW**



SIDE VIEW

DIMS IN MM.
ALL TOLERANCES ARE +/- 0.127
UNLESS OTHERWISE STATED.
NOT TO SCALE

Rev. 97 170809
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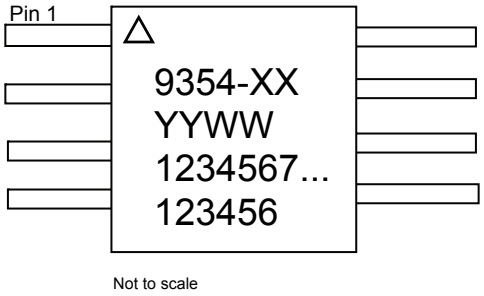
Figure 15. Top Marking Specifications



Not to scale

Line 1: Pin 1 indicator △ No e2v or Peregrine logos present
Line 2: Part number (XX will be specified by the purchase order)
Line 3: Date code (last two digits of the year and work week)
Line 4: Wafer lot # (as many characters as room allows)
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside symbolization on any of the Peregrine products.

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
9354-01*	PE9354 Engineering samples	8-lead CFP	50 / Tray
9354-11	PE9354 Flight units	8-lead CFP	50 / Tray
9354-00	PE9354 evaluation kit	Evaluation kit	1 / Box
8PCFP-MS	8 Pin Mechanical Samples	8 Pin CFP	1/Tray

Note: * The PE9354-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE9354-11 flight units. The PE9354-01 device provides the same functionality and footprint as the PE9354-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
e2v ~ http://www.tdehirel.com ~ inquiries@e2v-us.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. ***Preliminary Specification:*** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).