Determining Valid Divide Ratios Using Peregrine PLL Frequency Synthesizers

Introduction

The purpose of the N divider in a phase-locked loop (PLL) is to divide the high frequency of the VCO down to a more manageable frequency that the phase detector can process. Different architectures are available that use counters to scale the frequency. However, not every frequency can be realized due to restrictions with the counting registers. This application note describes how to determine which divide ratios are valid when using Peregrine Semiconductor's PLL frequency synthesizers.

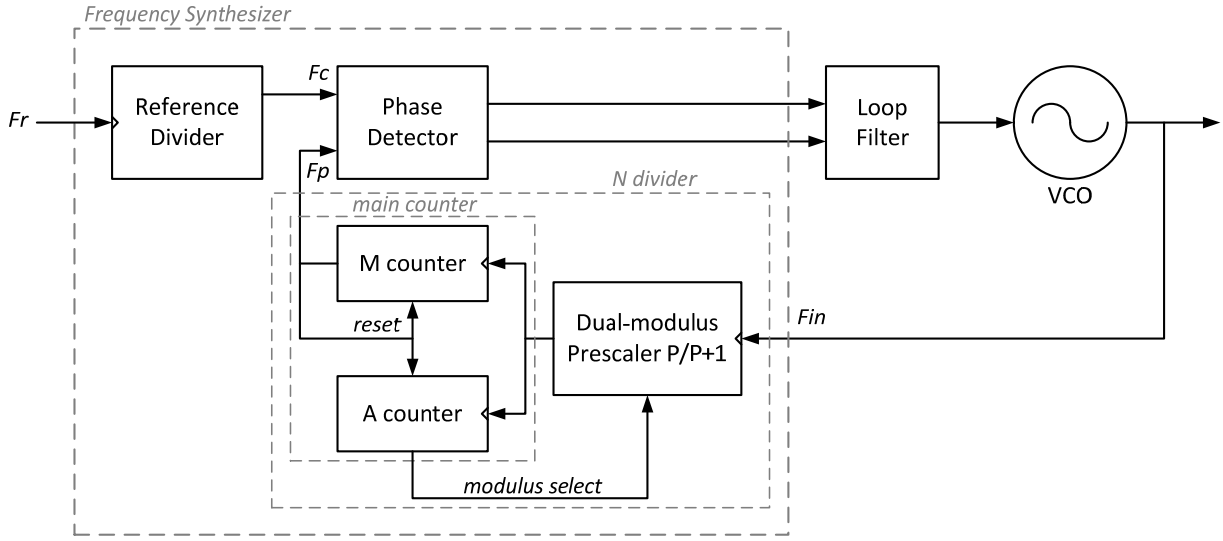
Summary

- A dual modulus prescaler cannot synthesize every frequency due to limitations with its architecture
- A selectable dual modulus prescaler with a lower modulus decreases the minimum continuous divide ratio and improves the frequency selectivity
- The valid divide ratio is further limited by the operational parameters of the noise shaping delta-sigma modulator of a fractional synthesizer
- Invalid divide ratios apply to M and A register values below N_{MIN}. Above N_{MIN} there is no limitation

Dual Modulus Prescaler

Frequency synthesizers can be integer-N or fractional-N depending on the design and requirements of the PLL. Both types of frequency synthesizers commonly use dual-modulus prescalers in the feedback (N) divider. Its architecture consists of a high frequency prescaler and two low frequency dividers as shown in *Figure 1*. The dual-modulus prescaler takes the high frequency of the VCO and divides it down to a more manageable lower frequency for the main counter. This configuration facilitates closer channel spacing with higher VCO frequency operation without losing the frequency resolution inherent in a single modulus N divider scheme.

Figure 1. Integer-N PLL Functional Block Diagram with a Dual Modulus Prescaler



The main counter chain then divides the prescaler output by an integer derived from the settings in the M and A counters. Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2." Therefore, the output from the main counter chain (F_P) is related to the VCO frequency (F_{IN}) by:

$$F_P = F_{IN} / [P * (M+1) + A] \quad (1)$$

where P is the lowest modulus value and

$$N = F_{IN} / F_P = P * (M+1) + A \quad (2)$$

$$M = N * (1/P) - 1 \quad (3)$$

where the integer value of M is used, and

$$A = N - P * (M + 1) \quad (4)$$

Integer-N Valid Divide Ratios

A dual modulus prescaler cannot synthesize every divide ratio due to the counting algorithm of the M and A counters. In order to guarantee a contiguous division ratio in integer mode, the following conditions must be met:

$$A \leq M + 1 \qquad (5)$$

$$N_{MIN} = P^2 - P \qquad (6)$$

The A counter can accept values as high as 15 when $N \geq N_{MIN}$, but in typical operation it will cycle from 0 to P – 1 in increments of M. Below N_{MIN}, some frequencies will not be attainable. If an invalid divide ratio is selected, the PLL may lock to the wrong frequency or lose lock completely.

As an example, for P = 10, contiguous channels will be achieved for $N \geq 90$. But suppose a divide ratio of 45 is needed to achieve a specific operating frequency such as 2.25 GHz using a comparison frequency of 50 MHz. Equations (3) and (4) determine the required register values:

M = 45 * (1/10) –1 = 3

A = 45 – 10 * (3+1) = 5

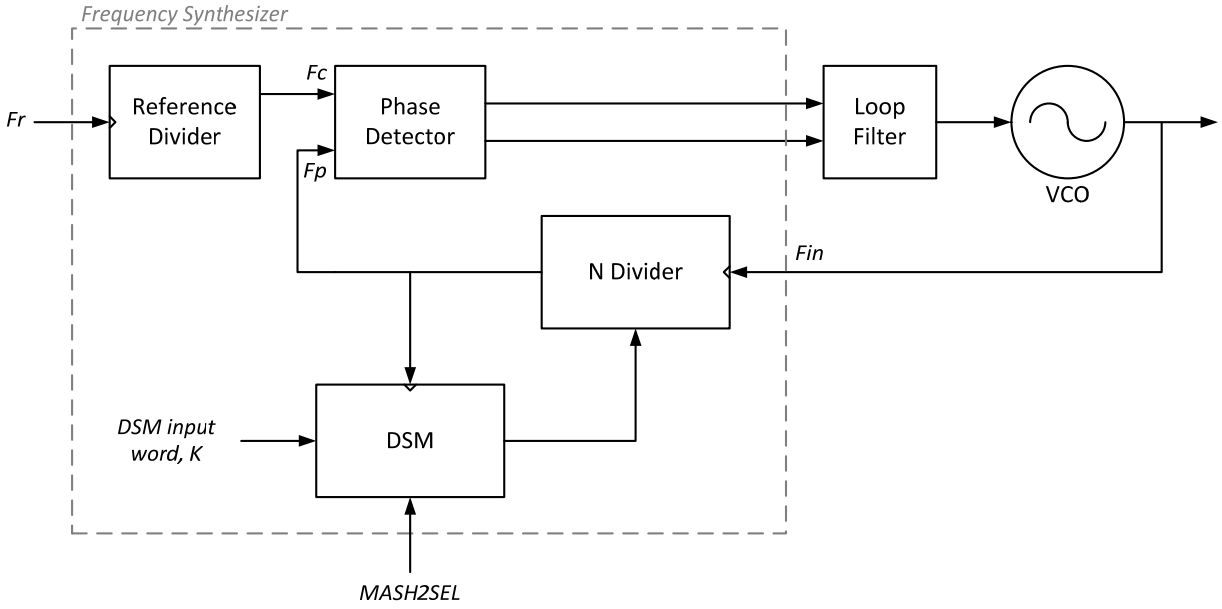
Since the $A \leq M + 1$ requirement is not met, 45 results in an invalid divide ratio using the allocated frequency plan. The comparison frequency could be scaled to another value such as 30 MHz, which would raise the divide ratio to 75. (Note that when scaling the comparison frequency while using the same loop bandwidth and VCO frequency, the theoretical change of in-band phase noise will be 10 * log (Fc1 / Fc2), where Fc1 is original and Fc2 the final frequency. Therefore, if Fc1 is 50 MHz and Fc2 is 30 MHz, the in-band floor noise will degrade by 2.2 dB.)

Lower contiguous divide ratios can be achieved by reducing the modulus value. Peregrine's next generation of PLL frequency synthesizers have selectable 5/6 and 10/11 dual-modulus prescalers. The 5/6 prescaler can achieve a minimum continuous divide ratio of 20. This would allow 45 to be a valid divide ratio in the previous example. Note that lowering the modulus requires the M and A counters to run at higher frequencies, which may exceed the limit of their capability. The maximum operating frequency of each prescaler mode is specified in the device datasheet.

Fractional-N Valid Divide Ratios

The integer-N frequency synthesizer is a widely used architecture, but its channel spacing or frequency step size is limited by the comparison frequency (F_C). In order to achieve a smaller step size, it is necessary to lower the comparison frequency, which results in a higher division ratio for the PLL, an increased in-band phase noise, lower loop bandwidth and slower switching speed. Fractional-N synthesizers allow the PLL to operate with a higher reference frequency while realizing a fine step size by periodically modulating the division ratio between N and N+1, for example, such that the average value contains a fractional element. This is the fundamental operation of the Delta-Sigma Modulator (DSM).

Figure 2. Peregrine Fractional-N PLL Functional Block Diagram



One of the consequences of the DSM is its generation of fractional spurs due to the accumulation of random phase errors. Delta-sigma noise shaping techniques are applied to fractional-N synthesizers to shift unwanted spurs outside the bandwidth of the loop filter. However, the valid divide ratio is further limited by the delta-sigma modulator due to variation of the instantaneous division ratio around the average correct division ratio.

Peregrine's PLL frequency synthesizers use two Multi-stAge noise Shaping (MASH) decimation structures for reducing fractional spurs. MASH-1-1 mode is a 2nd order fractional dithering using four (2^2) N values: N-1, N, N+1 and N+2. MASH-1-1-1 mode is a 3rd order fractional dithering using eight (2^3) N values: N-3, N-2, N-1, N, N+1, N+2, N+3 and N+4. MASH-1-1-1 mode reduces fractional spurs but decreases the number of valid programming frequencies.

In order to guarantee a contiguous division ratio in fractional operation, the following conditions must be met:

$$A \leq M + 1 \qquad (7)$$

MASH-1-1 mode:

$$N_{MIN} - 1 = (P^2 - P) \qquad (8)$$

MASH-1-1-1 mode:

$$N_{MIN} - 3 = (P^2 - P) \qquad (9)$$

Consider for example P = 10/11 and N = 90 using MASH-1-1 noise shaping. Because the desired divide ratio is below the minimum N value of 91 from equation (8), all four divide ratios must be verified against equation (7) as shown in *Table 1*:

Table 1. Determining Valid Divide Ratios in Fractional Mode

N	M	A	A ≤ M + 1?
N-1 = 89	7	9	invalid
N = 90	8	0	valid
N+1 = 91	8	1	valid
N+2 = 92	8	2	valid

Since the A ≤ M + 1 requirement is not met for all four values N-1 thru N+1, 90 cannot be used. However, choosing a different comparison frequency or selecting a lower modulus (if applicable), as described for the integer operation, may also be considered to achieve the desired operating frequency.

Conclusion

A dual modulus prescaler offers divider programmability and allows the frequency synthesizer to operate at higher frequencies without losing frequency resolution. However, it cannot synthesize every frequency due to limitations with its architecture. Having the ability to select a lower modulus decreases the minimum continuous divide ratio and improves the frequency selectivity. Fractional-N frequency synthesizers, using delta-sigma noise shaping techniques to reduce spurs, introduce an additional factor which further limits the valid N availability. Avoiding invalid divide ratios are necessary to ensure that the PLL will remain locked under normal operation.

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