



**PE9301**  
**EVALUATION KIT**  
**USER'S MANUAL**

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You may also contact us by fax or e-mail:

Fax: (858) 455-0770

E-Mail: [help@peregrine-semi.com](mailto:help@peregrine-semi.com)

## **FCC Labeling Requirement**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

# 1. Introduction

The PE9301 is a high performance 300Krad/s (Si) Total Dose; low power monolithic divider manufactured using Peregrine's UTSi CMOS process. It features a fixed divide ratio of 2 and can operate with input signals of up to 3.5 GHz. The PE9301 operates on a nominal 3 volts supply and draws only about 14 mA of current typical. Ideal for space microwave PLL synthesis solutions

# 2. Evaluation Board Description

The PE9301 evaluation board is depicted below in Figure 2. The input is driven into the RF In port while the divided output is taken at Out 1. Both input and output contain footprints for AC coupling capacitors (C3 and C1 respectively). The power supply connection is provided near the top of the evaluation board (J2) with the lower pin as the supply and the upper pin as ground. In addition C2, C5, and C10 are placeholders for power supply decoupling capacitors. Placeholders C4, C6, and C8 are needed for required bypass capacitors. **Note: C4 and C6 are located on the underside of the evaluation board.**

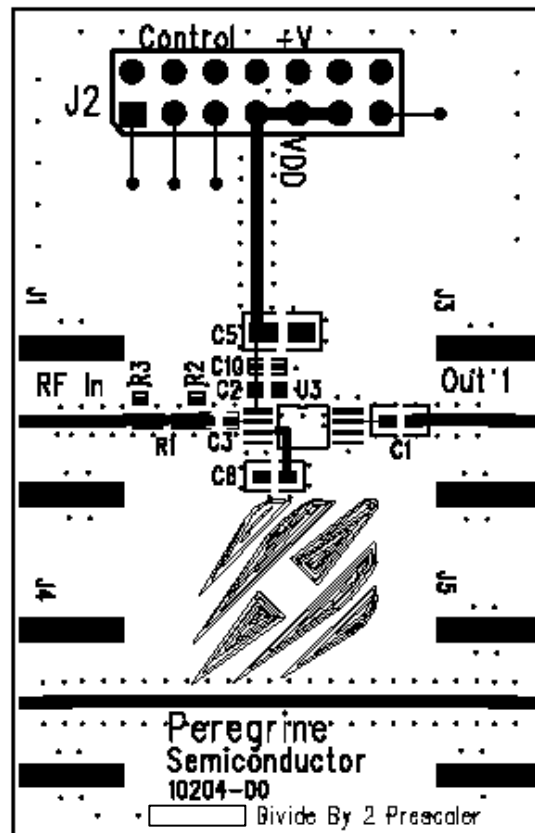
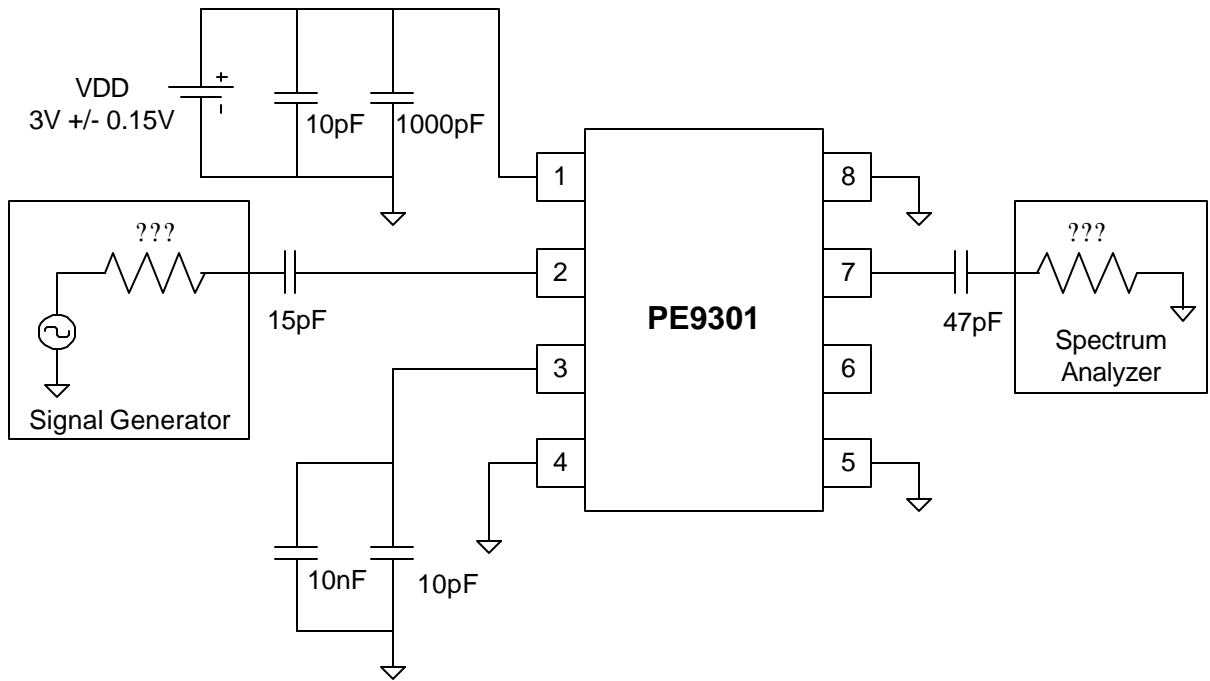


Figure 2. PE9301 Evaluation Board

### 3. Evaluation Board Test Setup

The PE9301 can be tested on the evaluation board using the test setup shown below in Figure 3. In the test setup, it is essential that the power supply is properly decoupled and bypass capacitors are used for pin 3. In addition, the input and output need to be AC coupled.

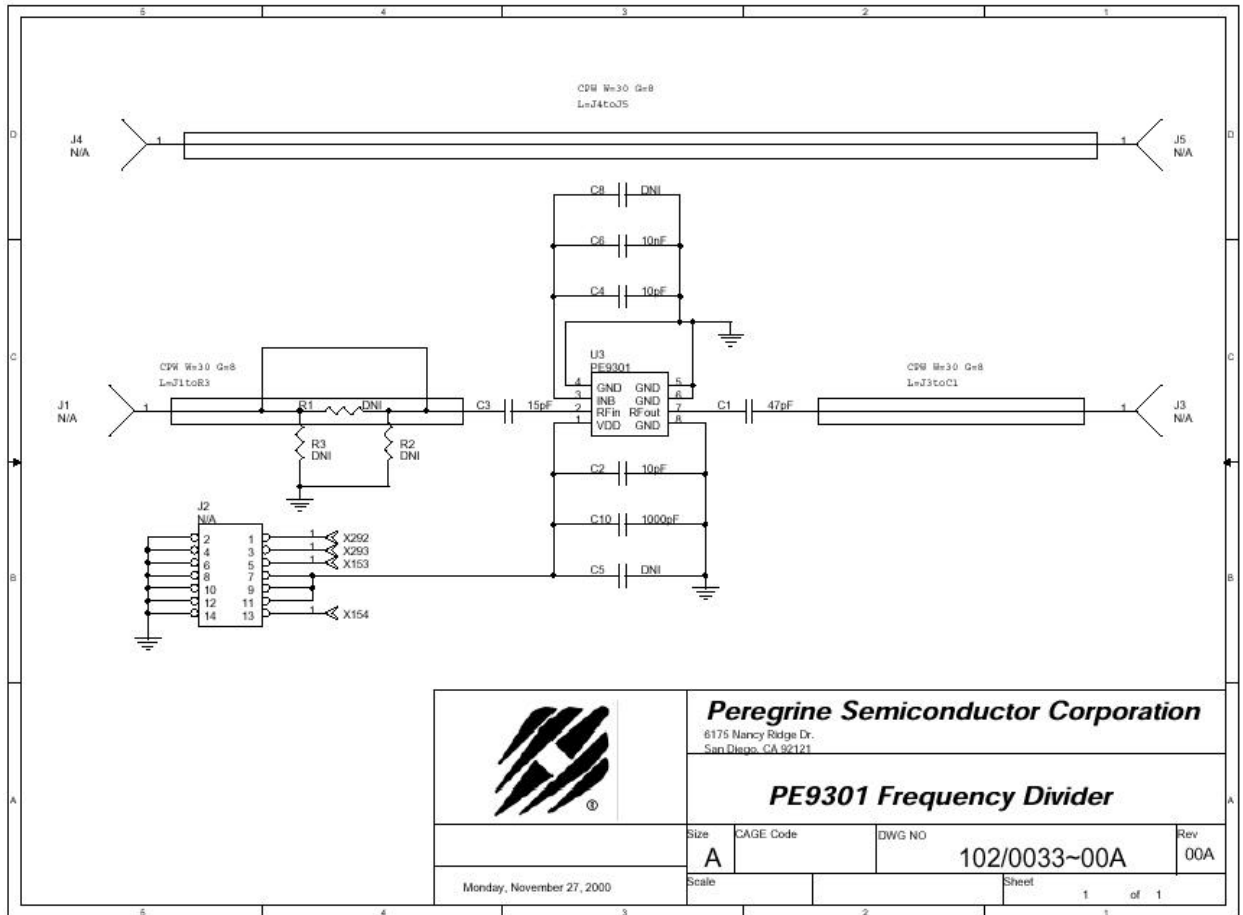



**Figure 3. PE9301 Test Setup**

## 4. Testing

The PE9301 Evaluation Board was measured prior to shipment using the setup depicted in figure 3. Testing was performed at room temperature and  $VDD = 2.85V$

The input sensitivity plot for the PE9301 board is included with the evaluation kit



	<b>Peregrine Semiconductor Corporation</b> 6175 Nancy Ridge Dr. San Diego, CA 92121			
	<b>PE9301 Frequency Divider</b>			
Monday, November 27, 2000	Size <b>A</b>	CAGE Code	DWG NO <b>102/0033~00A</b>	Rev <b>00A</b>
	Scale		Sheet <b>1</b>	of 1

PE9301 Frequency Divider Revised: Monday, November 27, 2000					
102/0033~00A		Revision: 00A			
Peregrine Semiconductor Corporation					
6175 Nancy Ridge Dr.					
San Diego, CA 92121					
Bill Of Materials		November 27,2000		10:03:57	
Item	Quantity	Reference	Value	Part Description	Notes
1	1	C1	47pF	SMD CAP 0603	
2	2	C2,C4	10pF	SMD CAP 0402	
3	1	C3	15pF	SMD CAP 0402	
4	1	C5	DNI	SMD CAP 0805	
5	1	C6	10nF	SMD CAP 0402	
6	1	C8	DNI	SMD CAP 0603	
7	1	C10	1000pF	SMD CAP 0402	
8	4	J1,J3,J4,J5	N/A	SMA Connector (Side Mount)	
9	1	J2	N/A	Header 14	
10	3	R1,R2,R3	DNI	Not used	
11	1	U3	PE9301	Divide by 2	
12	4	X153,X154,X292,X293	T POINT A		