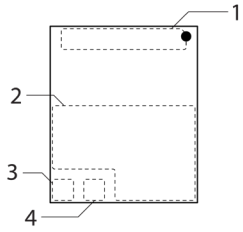
TDG650E30BEP
Bottom-side cooled 650 V E-mode GaN transistor
Product Specification

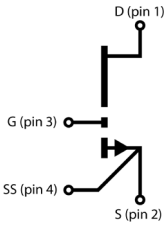
Features

- **650 V enhancement mode power transistor**
- **Bottom-side cooled configuration**
- **RDS(on) = 50 mΩ**
- **IDS(max) = 30 A**
- **Ultra-low FOM Island Technology® die**
- **Low inductance GaNPX® package**
- **Easy gate drive requirements (0 V to 6 V)**
- **Transient tolerant gate drive (-20 V / +10V)**
- **Very high switching frequency (> 100 MHz)**
- **Fast and controllable fall and rise times**
- **Reverse current capability**
- **Zero reverse recoveryloss**
- **Small 7.1 x 8.5 mm² PCB footprint**
- **Source Sense (SS) pin for optimized gatedrive**
- **RoHS 6 compliant**

Package Outline



Circuit Symbol



Applications

- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Motor Drives
- Solar and Wind Power
- Fast Battery Charging
- On Board Battery Chargers
- E-Switch

Description

The TDG650E30BEP is an enhancement mode GaN-on-silicon power transistor based on GaN Systems Technology. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. Teledyne e2v implements patented **Island Technology®** cell layout for high current performance and yield. **GaNPX®** packaging enables low parasitic inductance & low thermal resistance in a small package.

The Teledyne e2v TDG650E60BEP is a bottom-side cooled transistor that offers very low junction-to- case thermal resistance for demanding high power applications. These features combined provide very high efficiency power switching..

Table 1 Absolute Maximum Ratings (Tcase = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Step Stress Gate-to-Source Voltage (Tj=175°C,12h) [4]	STSVgs	8	V
Continuous Drain Current (T_{case} = 25 °C) (note 2)	I_{DS}	30	A
Continuous Drain Current (T_{case} = 100 °C) (note 2)	I_{DS}	25	A
Pulse Drain Current (Pulse width 50 µs, VGS=6V) (note 3)	$I_{DS\ Pulse}$	60	A

(1) For ≤ 1 µs, Non repetitive
(2) Limited by saturation
(3) Defined by product design and characterization. Value is not tested to full current in production.
(4) Please contact Teledyne e2v for additional Information regarding Step Stress

Table 2 Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.5	°C /W
Thermal Resistance (junction-to-ambient) (note 5)	$R_{\Theta JA}$	24	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(5) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Table 3 Ordering Information

Ordering code	Package type	Packing method	Qty	Part Marking	Origin	ECCN
TDG650E30BEP	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	TDG630BE	US	EAR99
TDG650E30BEPF	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	TDG630BF	EU	EU

Table 4 Electrical Characteristics

Typical values at TJ = 25 °C, VGS = 6 V. Unless otherwise noted, Min/Max values are specified over the full temperature range from TJ = -55 °C to TJ = 150 °C based on Teledyne Dynamic Burn-In[5] after 15k Cycles.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V, I_{DSS} = 50 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		50	63	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 9 A
Drain-to-Source On Resistance (After Stress)	$R_{DS(on)}$		**53**	80	mΩ	Based on Life Testing at Max Conditions, Reading @ Tj=25°C
Drain-to-Source On Resistance	$R_{DS(on)}$		150		mΩ	V_G = 6 V, T_J = 150 °C I_{DS} = 9 A
Dynamic Drain-to-Source On Resistance Shift	$DR_{DS(on)}$		25	30	%	V_{GS}=6v I_{DS}=9 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 7 mA
Gate-to-Source Current	I_{GS}		160		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V, I_{DS} = 30 A
Drain-to-Source Leakage Current	I_{DSS}		2	50	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		400		µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 150 °C
Internal Gate Resistance	R_G		1.1		Ω	f = 25 MHz, open drain
Input Capacitance	C_{ISS}		242		pF	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		65		pF	
Reverse Transfer Capacitance	C_{RSS}		1.5		pF	
Effective Output Capacitance, Energy Related (note 5)	$C_{O(ER)}$		100		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance, Time Related (note 6)	$C_{O(TR)}$		160		pF	
Total Gate Charge	Q_G		6.1		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		1.7		nC	
Gate-to-Drain Charge	Q_{GD}		2.2		nC	
Output Charge	Q_{OSS}		64		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(6) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}
(7) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Table 5 Electrical Characteristics cont'd (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		4.1		ns	V_{DD} = 400 V, V_{GS} = 0-6 V I_{DS} = 16 A, $R_{G(ext)}$ = 5 Ω T_J = 25 °C (note 7)
Rise Time	t_R		3.7		ns	
Turn-Off Delay	$t_{D(off)}$		8		ns	
Fall Time	t_F		5.2		ns	
Turn-On Delay	$t_{D(on)}$		4.3		ns	V_{DD} = 400 V, V_{GS} = 0-6 V I_{DS} = 16 A, $R_{G(ext)}$ = 5 Ω T_J =125 °C (note 7)
Rise Time	t_R		4.9		ns	
Turn-Off Delay	$t_{D(off)}$		8.2		ns	
Fall Time	t_F		3.4		ns	
Output Capacitance Stored Energy	E_{OSS}		7		µJ	V_{DS} = 400 V V_{GS} = 0 V, f = 1 MHz
Switching Energy during turn-on	E_{on}		47.5		µJ	V_{DS} = 400 V, I_{DS} = 15 A V_{GS} = 0 - 6 V, $R_{G(on)}$ = 10 Ω $R_{G(off)}$ = 1 Ω, L = 40 µH L_P = 10 n (notes 8,9)
Switching Energy during turn-off	E_{off}		7.5		µJ	

(8) See Figure 17 for timing test circuit diagram and definition waveforms
(9) LP = parasitic inductance
(10) See Figure 18 for switching test circuit

Electrical Performance Graphs

Figure 1 I_{DS} vs. V_{DS} Characteristic

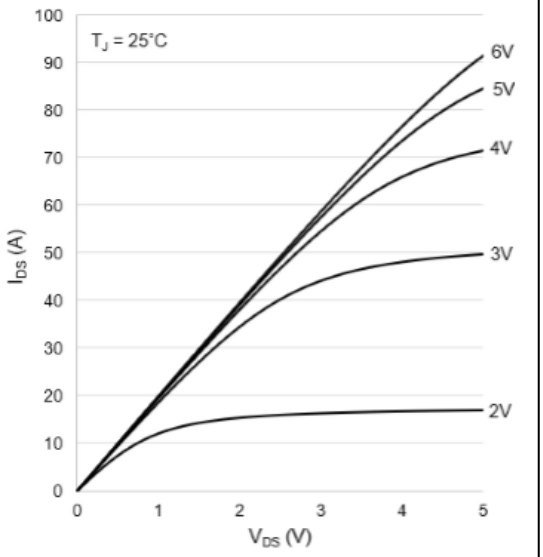


Figure 2 I_{DS} vs. V_{DS} Characteristic

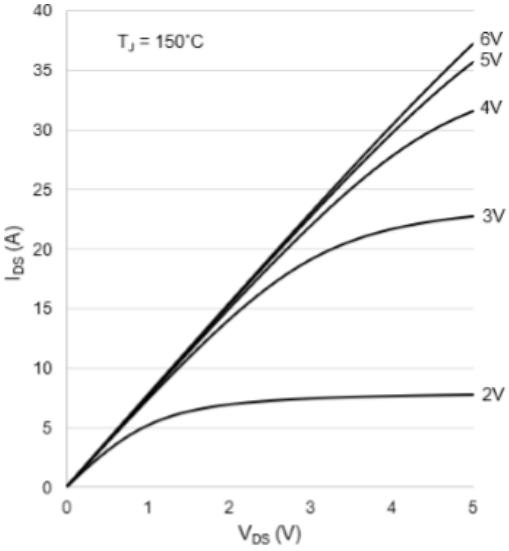


Figure 3 $R_{DS(on)}$ vs. I_{DS} Characteristic

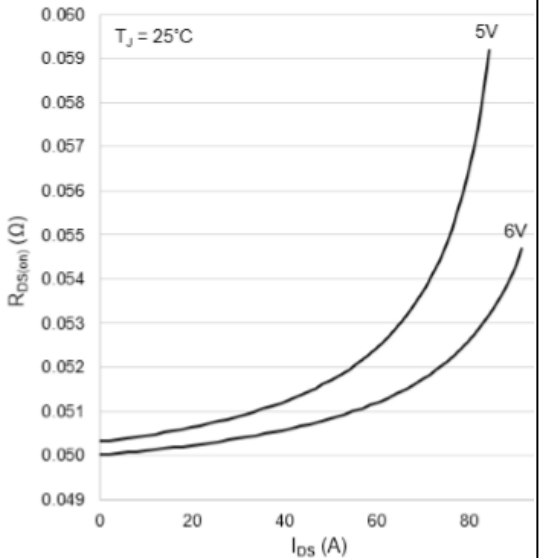
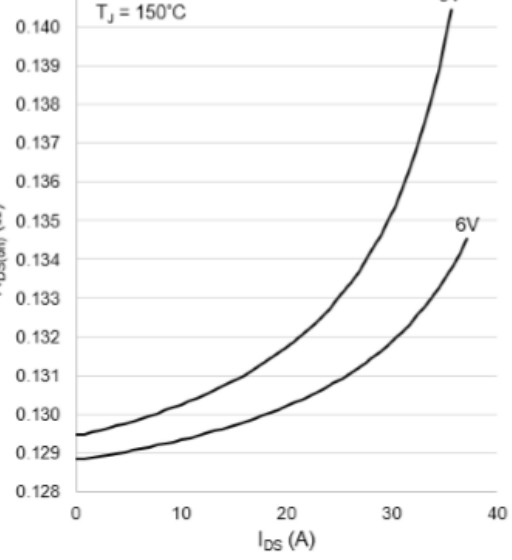


Figure 4 $R_{DS(on)}$ vs. I_{DS} Characteristic



Electrical Performance Graphs (continued)

Figure 5 I_{DS} vs. V_{DS}, T_J dependence

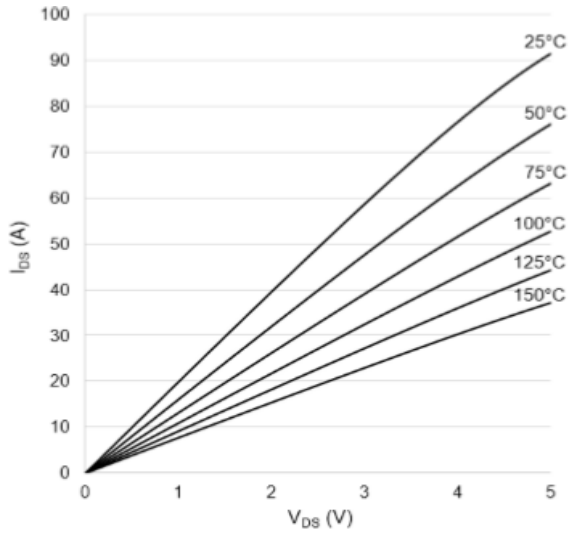


Figure 6 Gate Charge, Q_G Characteristic

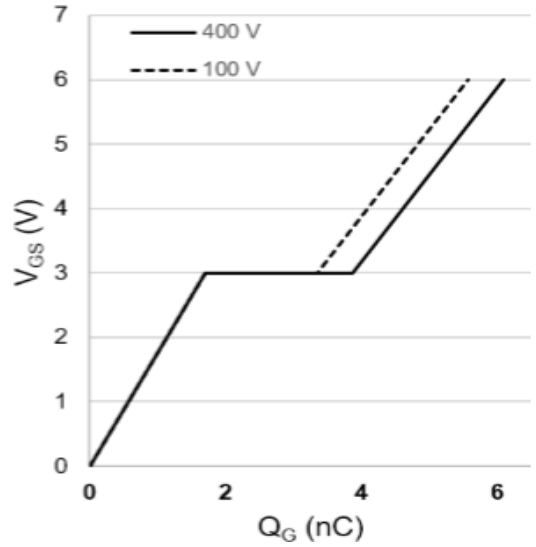


Figure 7 Capacitance Characteristics

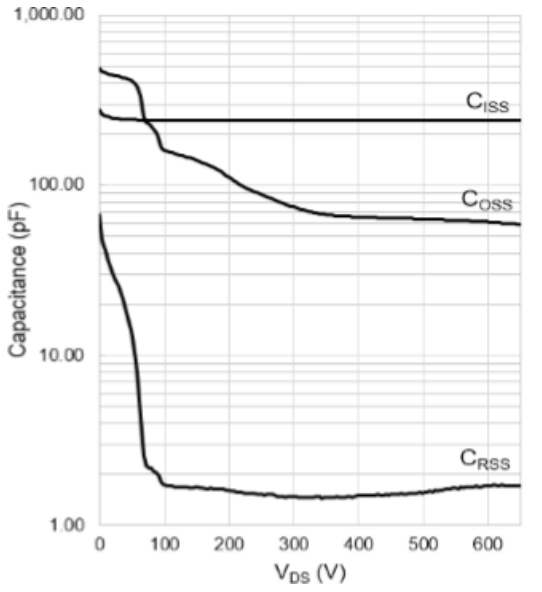
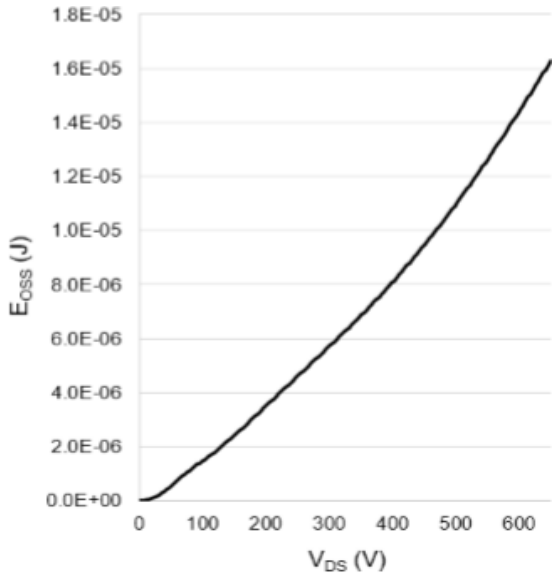


Figure 8 Stored Energy Characteristic



Electrical Performance Graphs (continued)

Figure 9 Reverse Conduction Characteristics Typical ISD vs. VSD @ TJ = 25 °C

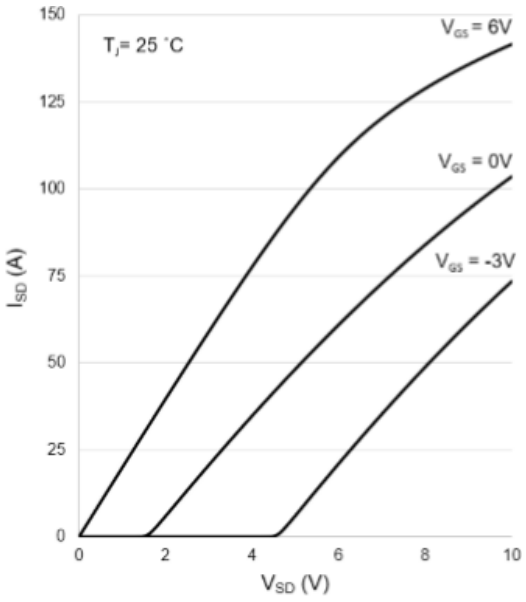


Figure 10 Reverse Conduction Characteristics Typical ISD vs. VSD @ TJ = 150 °C

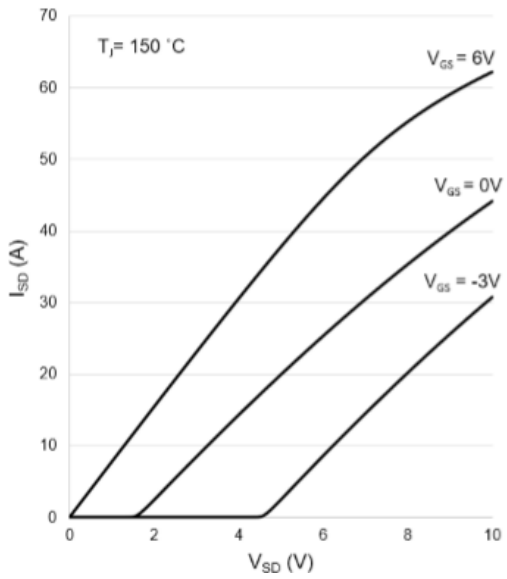


Figure 11 IDS vs. VGS Characteristic

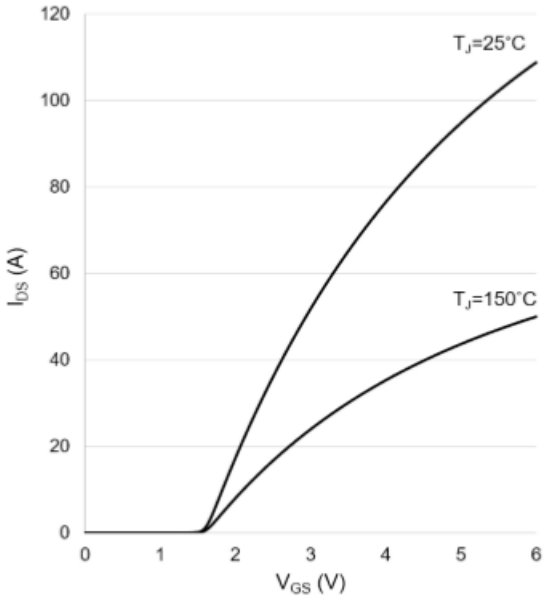
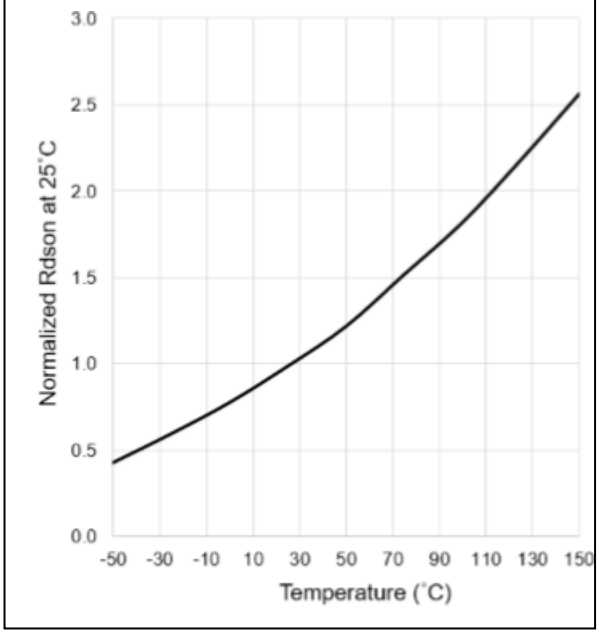


Figure 12 RDS(on) TJ Temperature Dependence



Thermal Performance Graphs

Figure 13 I_{DS} - V_{DS} SOA (T_{CASE}=25°C)

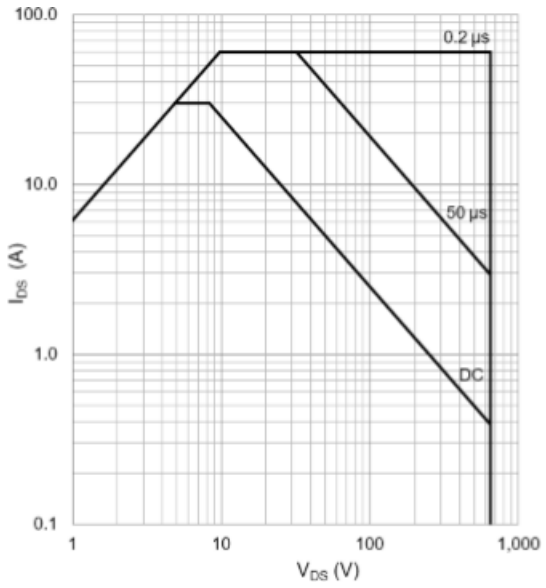


Figure 14 I_{DS} - V_{DS} SOA (T_{CASE}=125°C)

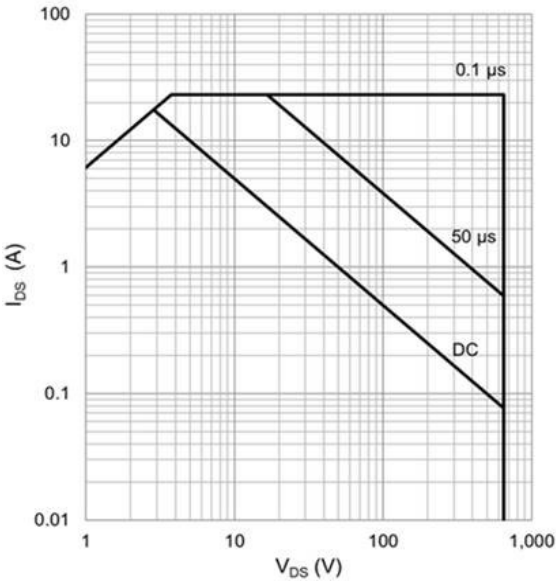


Figure 15 Power Dissipation Temperature Derating

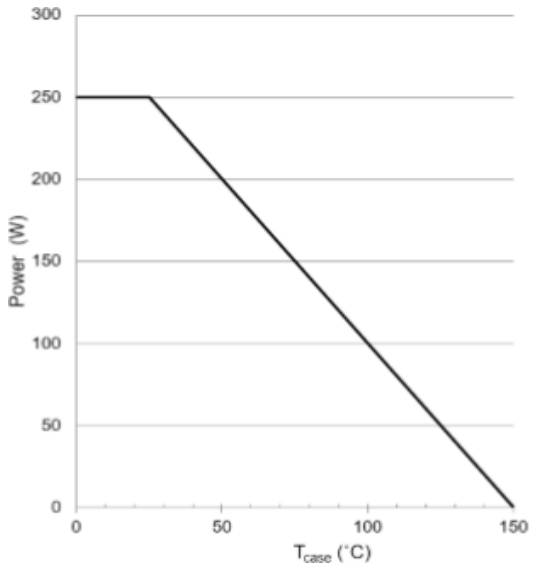
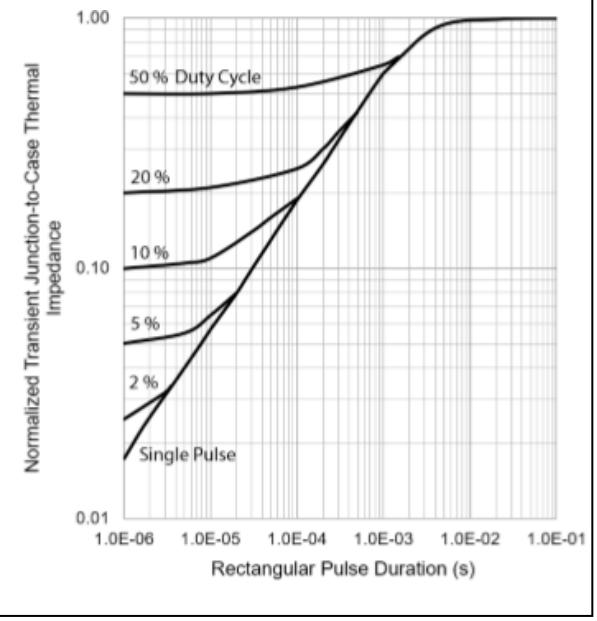


Figure 16 Transient RθJC



Test Circuits

Figure 17 TDG650E30BEP switching time test circuit and waveforms

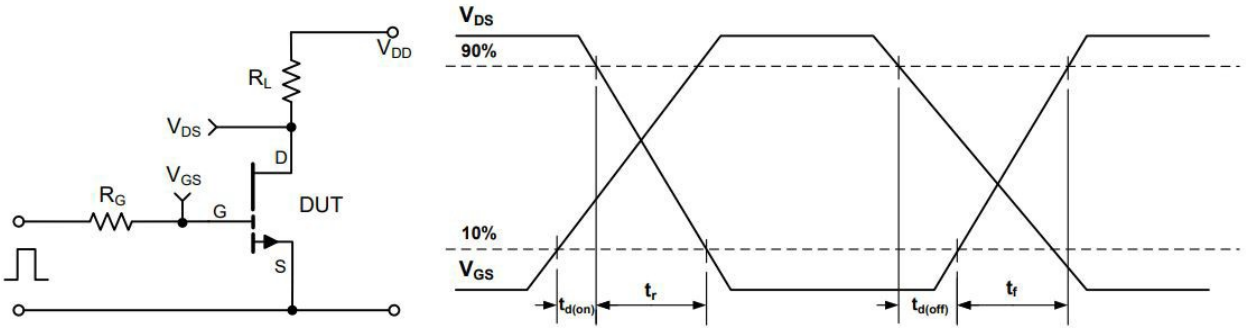
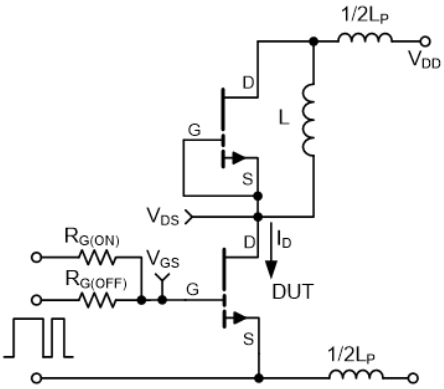


Figure 18 TDG650E30BEP Switching Loss Test Circuit



Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 7 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, Teledyne E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 at www.gansystems.com.

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. Teledyne E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

The TDG650E30BEP has a dedicated source sense pin. The GaN*PX*® packaging utilizes no wire bonds so the source connection is very low inductance. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved connecting the gate drive signal from the driver to the gate pad on the TDG650E30BEP and returning from the source sense pad on the TDG650E30BEP to the driver ground reference.

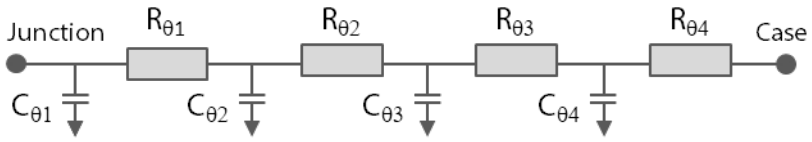
Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the TDG650E30BEP. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

TDG650E30BEP RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.015	$C_{\theta 1}$ = 8.0E-05
$R_{\theta 2}$ = 0.23	$C_{\theta 2}$ = 7.4E-04
$R_{\theta 3}$ = 0.24	$C_{\theta 3}$ = 6.5E-03
$R_{\theta 4}$ = 0.015	$C_{\theta 4}$ = 2.0E-03

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*™ Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

Teledyne enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for Teledyne transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a Teledyne enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for 1 µs is acceptable.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the TDG650E30BEP device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

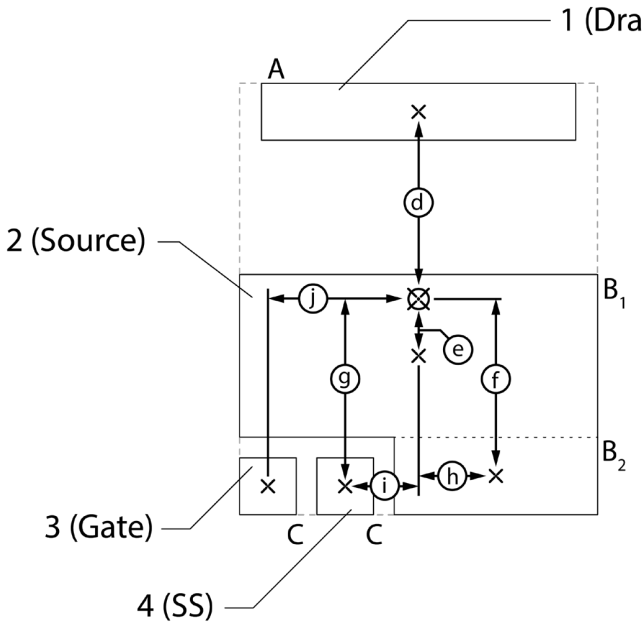
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues.

Recommended PCB Footprint for TDG650E30BEP



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	6.10	1.10	0.240	0.043
B_1	6.95	3.15	0.274	0.124
B_2	3.95	1.50	0.156	0.059
C	1.10	1.10	0.043	0.043

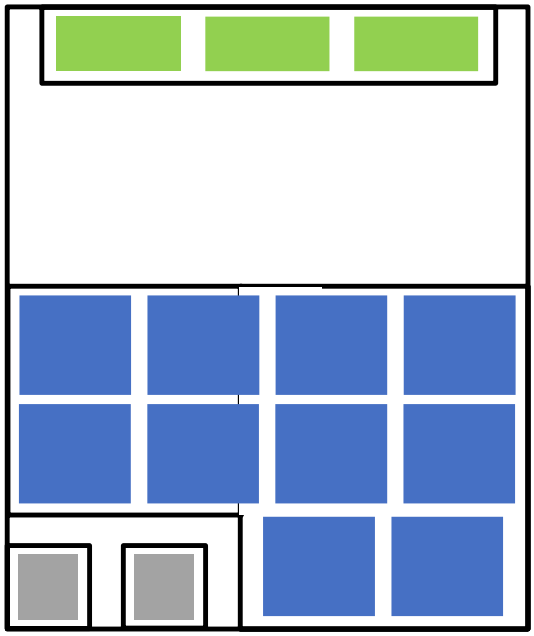
Dimensions

	mm	Inches
d	3.63	0.143
e	1.10	0.043
f	3.43	0.135
g	3.63	0.143
h	1.50	0.059
i	1.42	0.056
j	2.93	0.115

PCB pad openings

Package outline

Recommended Solder Stencil for Bottom-side Cooled PCB Footprint



Dimension of the Stencil Aperture

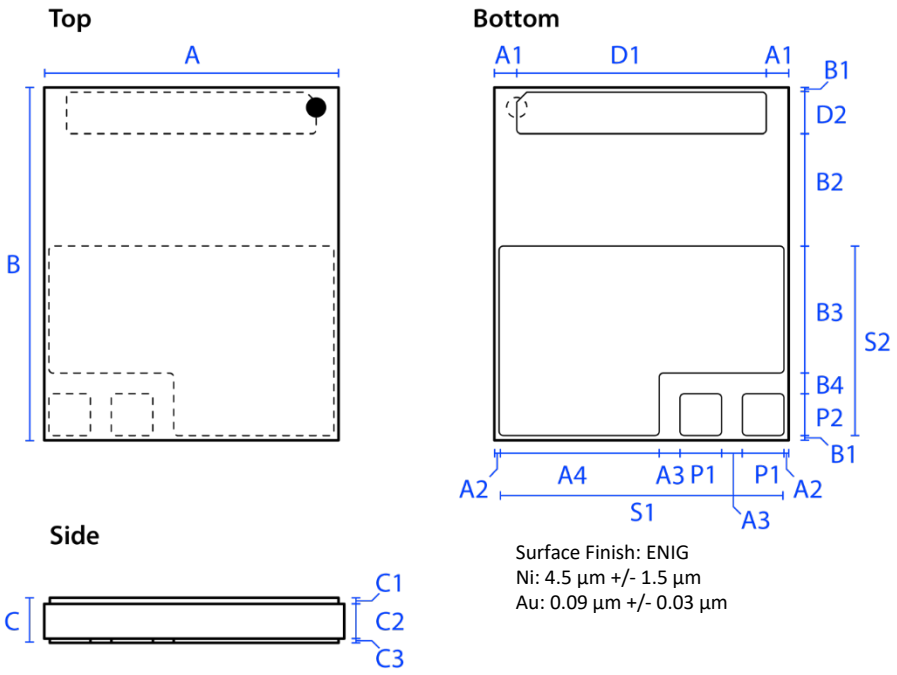
0.84 x 0.84 mm

1.75 x 0.8 mm

1.5 x 1.3 mm

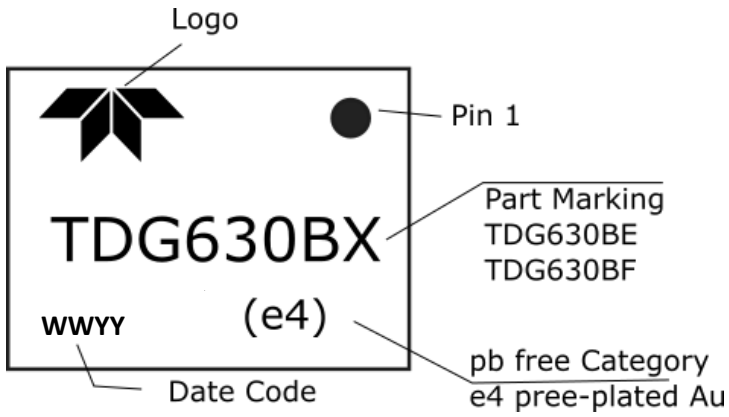
- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

Package Dimensions

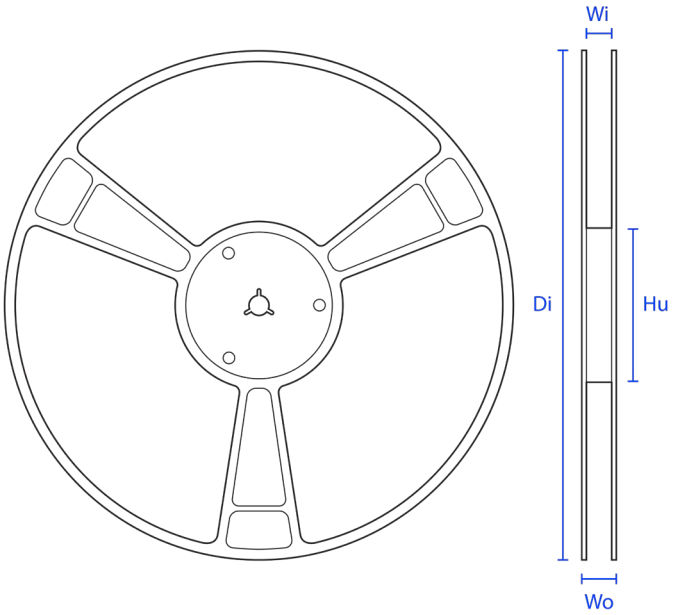


Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

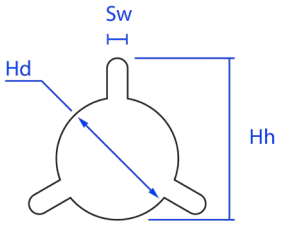
	mm	
	Max	Min
A	7.10	6.88
A1	0.565	0.415
A2	0.165	0.015
A3	0.55	0.45
A4	3.875	3.775
B	8.50	8.28
B1	0.165	0.015
B2	2.75	2.65
B3	3.10	3.00
B4	0.55	0.45
C	0.56	0.372
C1	0.045	0.026
C2	0.45	0.338
C3	0.031	0.011
D1	6.05	5.95
D2	1.025	0.925
P1	1.05	0.925
P2	1.025	0.925
S1	6.85	6.75
S2	4.575	4.475



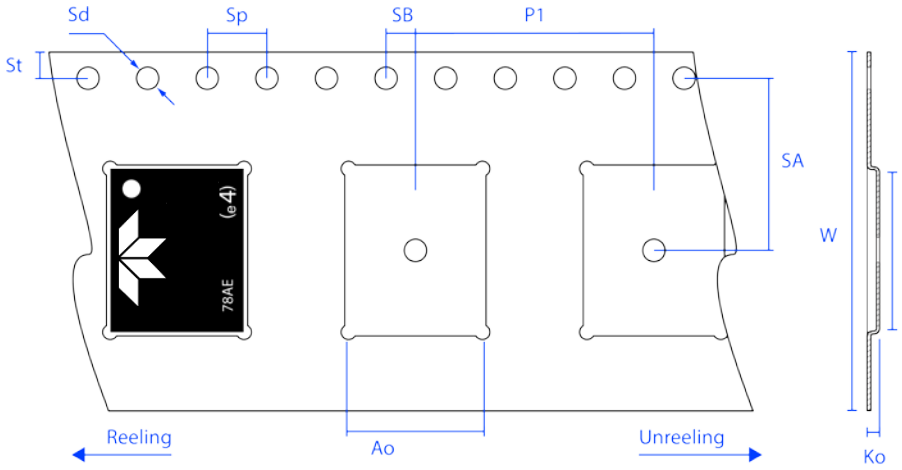
GaN*PX*® Part Marking



Dimensions (mm)				
	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	180.0	+1.5 / - 2.0
Wo	22.4	MAX	22.4	MAX
Wi	16.4	+ 2.0 / - 0.0	16.4	+ 2.0 / - 0.1
Hu	100.0	+/- 1.5	60.0	+ 2.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.8
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.1	+/- 0.3



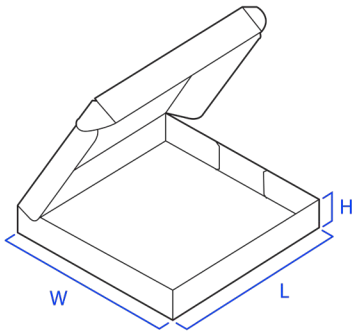
Note: Wo and Wi measured at hub



Dimensions (mm)		
	Nominal	Tolerance
P1	16.00	+/- 0.1
W	24.00	+ 0.3 / - 0.1
Ko	1.14	+/- 0.1
Ao	9.48	+/- 0.1
Bo	11.43	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	11.50	+/- 0.1
SB	2.00	+/- 0.1

TDG650E30BEP GaN*PX*® Tape and Reel Information

Tape and Reel Box Dimensions



Outside dimensions (mm)		
	7″ mini-reel	13″ tape-reel
W	197	342
L	204	355
H	32	53

Document Categories

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

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