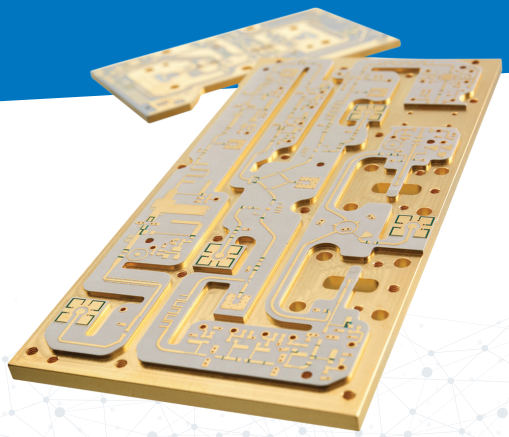
Thermal Management in High Performance RF and Microwave PCBs



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Introduction

As new RF and microwave systems evolve, we are seeing a greater need for effective thermal management and significantly higher RF performance from Printed Circuit Boards (PCB's) and subsystems; at the same time these systems are required to decrease in mass and still offer greater functionality than ever before. Constraints like these are often most acute in applications where Size, Weight and Power (SWaP) are high priorities such as military and aerospace and typically include RF power amplifiers and phased array TxRx modules. This paper reviews the various methods of thermal management and reviews in detail the advantages of "Coin" technology versus traditional thermal via technology.

High density active power devices, such as GaN power transistors, can dissipate significant heat. One of many roles that the PCB has to perform is to channel heat from the underside of the semiconductor device through to the chosen heatsinking scheme as efficiently and effectively as possible. The design challenge is how best to accomplish this while achieving the other trade-offs required such as RF performance, manufacturability and cost.

Methods of Thermal Management

Traditionally designers have simply added plated through holes (PTHs) to thermal/ground pads under components to take heat away through the circuit to a thermal sink such as a cold wall. Unless the assembly process includes a step to pre-fill these PTHs with solder there is a high risk that solder will be robbed from under the component into the holes leading to a poor and potentially unreliable connection. Another solution often used is to have these PTHs under the components filled with a proprietary via plugging paste and plated over the top to give an uninterrupted ground pad. The plugging pastes typically used are electrically non-conductive and offer a relatively low thermal conductivity of around 0.6 W/mK compared to a conductivity of copper of 400 W/mK, so do not contribute much to the thermal transfer. Electrically and thermally conductive paste, for example silver (Ag) loaded epoxy, can be used to fill the thermal PTHs but even with Ag epoxy the thermal conductivity of these pastes is typically in the range of 4 to 30 W/mK depending upon type - still very low. Figure 1 a) shows an example of a cross section though a filled and over-plated via. Figure 1 b) shows a typical application with filled thermal vias within the ground pad. If you look closely you will notice subtle outlines of the thermal vias in the central large ground pad.

To improve thermal conductivity one option is to increase the plated wall thickness of the PTHs from the standard 25um, to 100um for example. Often a greater number of smaller PTHs within a ground pad can provide a more effective thermal path than fewer larger PTHs.

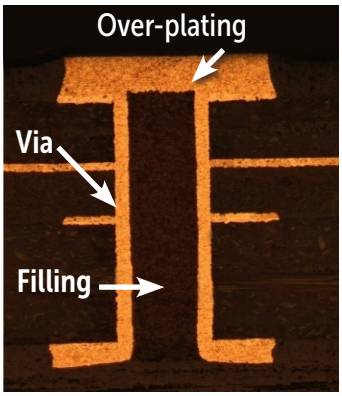


Figure 1: a) Cross-section of filled via

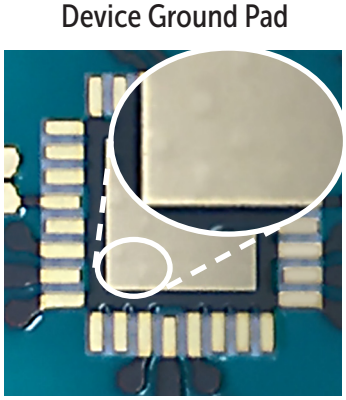


Figure 1: b) photo of typical device ground pad with over-plated vias just visible

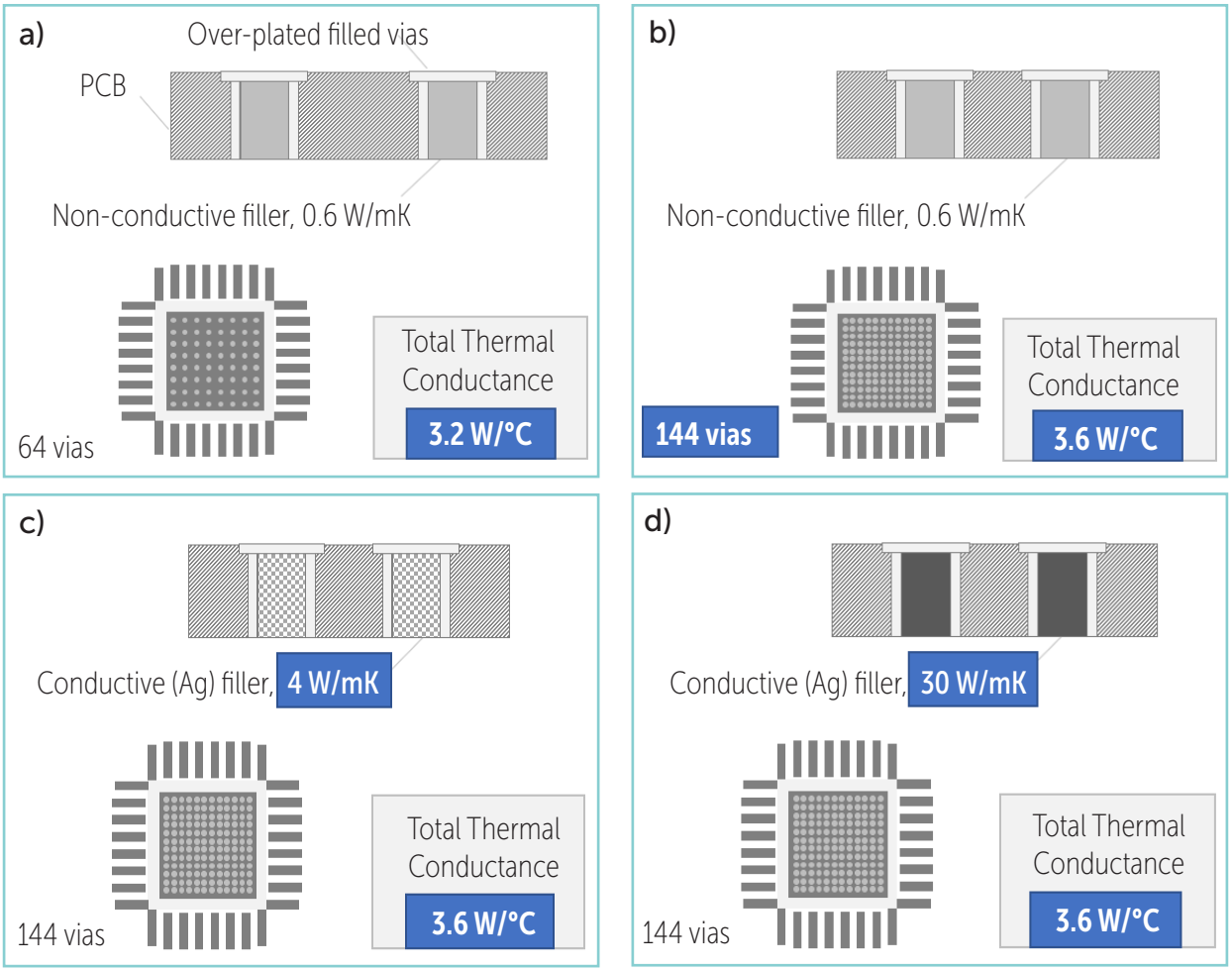


Figure 2: Comparison of total thermal conductance of different filled vias

There are limits to the effectiveness of heat transfer using a traditional ground pad with PTHs. Figure 2 shows the results of calculations of four different cases, with detailed calculations shown in Appendix 1. Starting with a typical case of PTHs with 0.1mm thickness of wall plating[1], it examines the overall thermal conductance with vias filled with a non-conductive filler (Figure 2 a)). Using this as the base case, it then examines increasing the number of vias (Figure 2 b)), then changes the filling from non-conductive to conductive silver epoxy of two different thermal conductivities (Figure 2 c) and d)). As can be seen the benefit of using Ag epoxy instead of standard non-conductive plug paste to fill the vias is limited and generally not worth the additional expense.

[1] While a through-hole wall thickness of 0.025mm is standard in non-thermally challenged applications, we usually recommend 0.1mm where heat transfer is important. Note that if standard 0.025mm plating was used for case 2a, then thermal conductance would only be 0.96 W/°C.

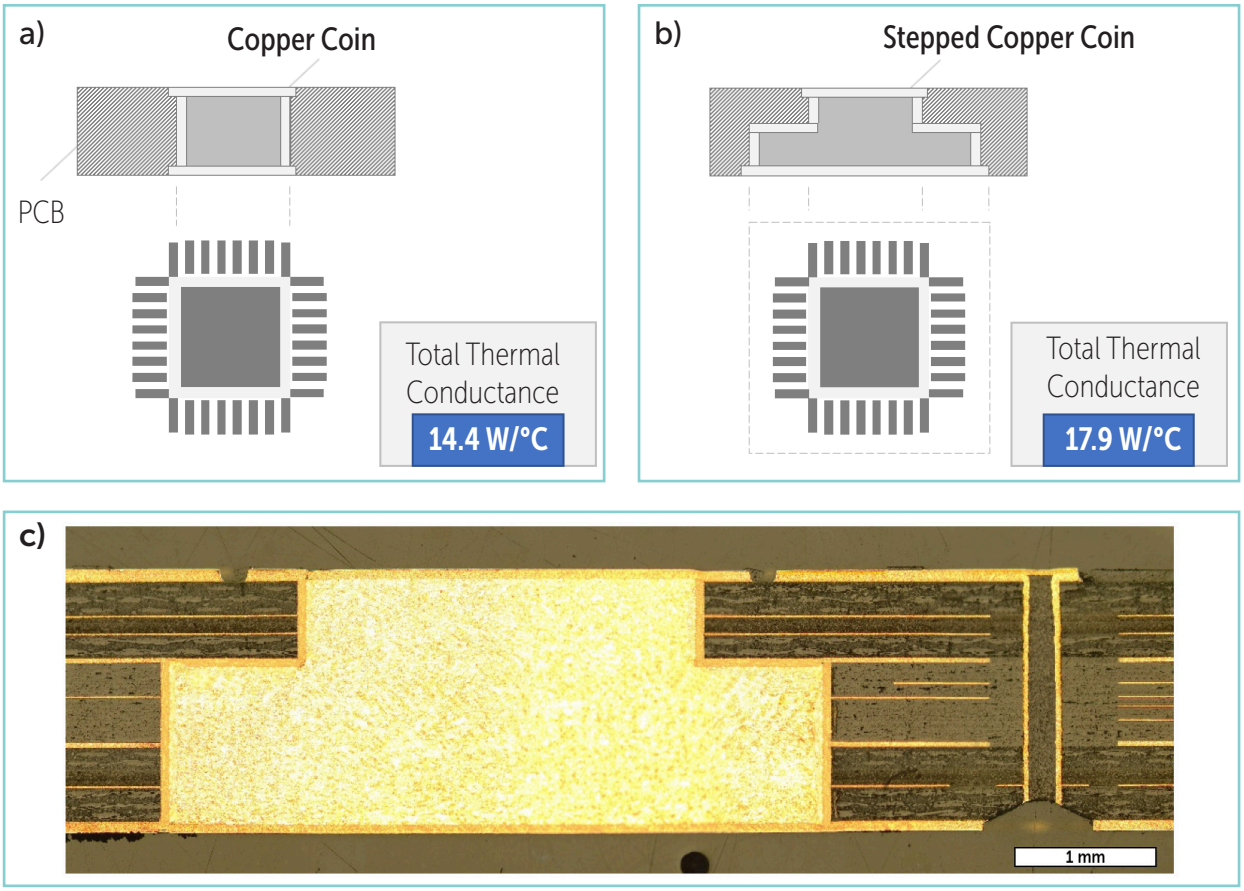


Figure 3: Examples of the use of copper coins

For many leading edge applications the total thermal conductances shown on previous page are not up to the task. A more effective approach is to use copper coins that are integrated into the circuit's structure. For ease of comparison, a simple approach is shown in (Figure 3 a)), where a 6mm x 6mm square coin is modelled. A more frequently used approach is to have the coin stepped so that heat is not only efficiently conducted away but also spread. This is modelled in (Figure 3 b)), and a cross sectional photograph of a real stepped copper coin shown in (Figure 3 c)). The larger area of copper provides a larger surface area in contact with the cold wall, providing improved thermal transfer. More detailed calculations are given in Appendix 2.

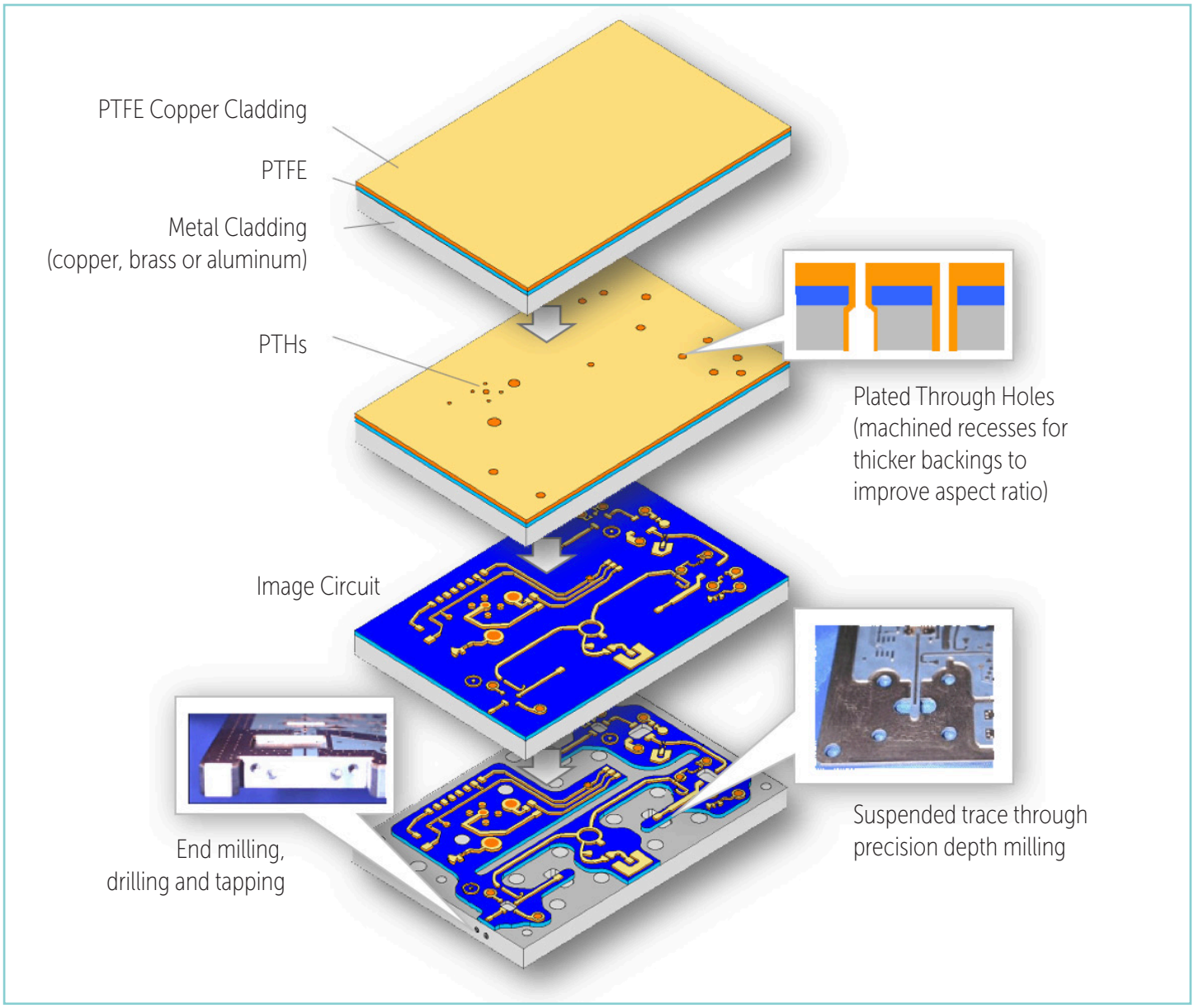


Figure 4: construction of metal-backed circuits

Ultimately metal backed circuits offer an ideal solution where large amounts of thermal energy need to be dissipated, as shown in Figure 4. The metal backing can be copper, aluminium or brass as this type of circuit is typically used for solid state power amplifiers (SSPA) and can be of either pre-bonded or post bonded structure. In the case of pre-bonded circuits this is where the substrate is supplied pre-bonded to a thick metal backer. This does limit tracking to a single layer and presents issues during processing as invariably machining operations have to take place after the circuit traces have been formed. Great care needs to be taken to avoid damaging critical circuit features. The advantage is that this provides an excellent ground plane reference.

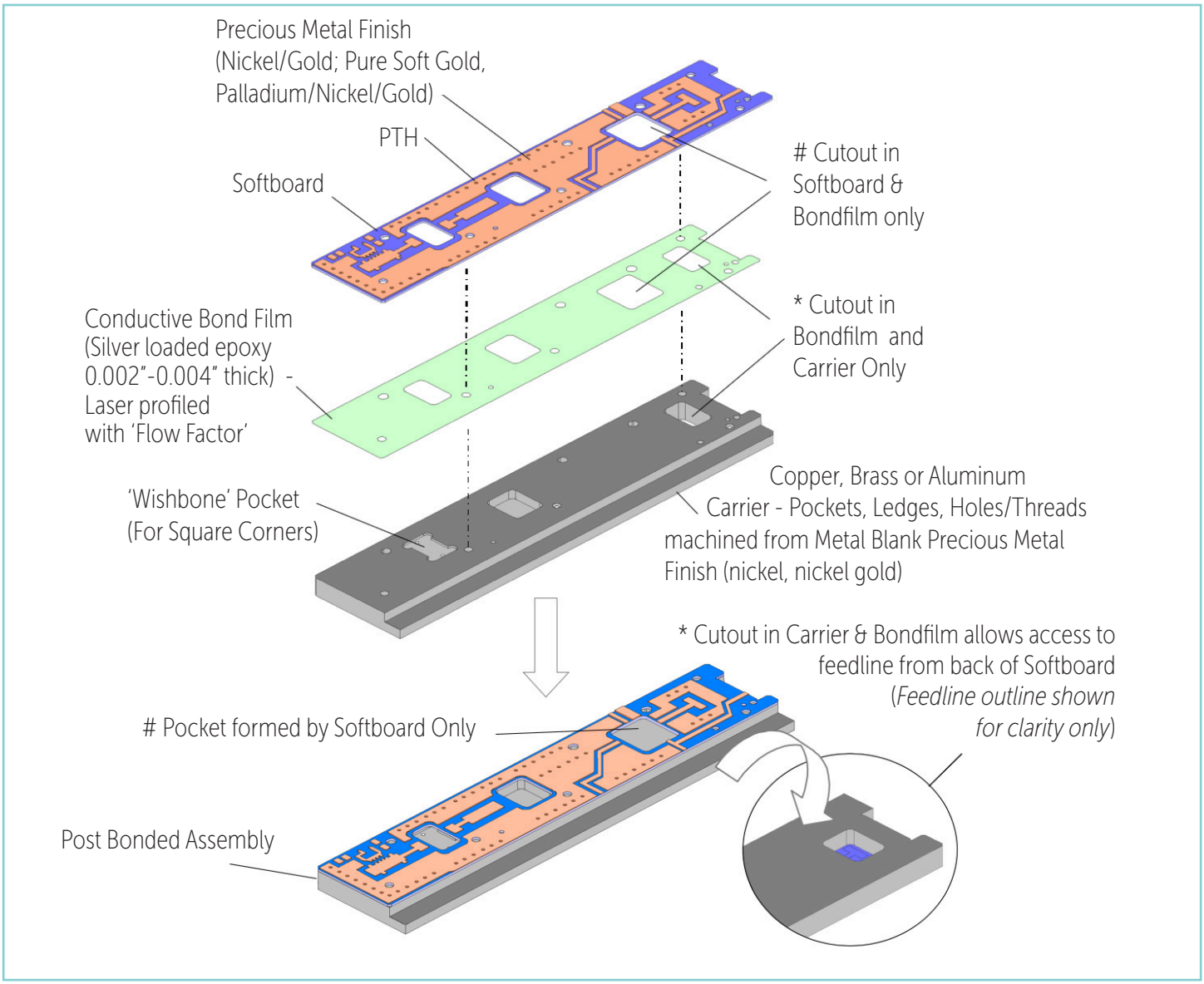
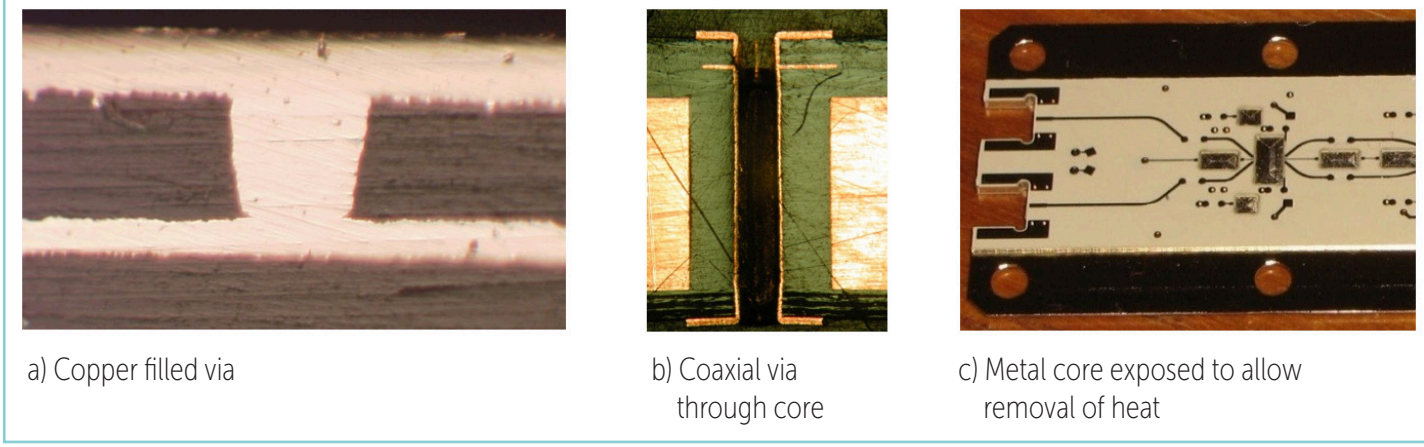


Figure 5: The assembly of post-bonded circuits

The post bonded alternative is easier to manufacture in so much as the circuit is produced and verified before being attached to a pre-machined and plated metal backer as shown in Figure 5. Post bonded circuits can have more than a single layer of conductors. Generally the circuit is bonded to the metal backer using a conductive adhesive layer. For both pre and post bonded circuits the components that require heat to be transferred away are mounted directly onto the metal backer through openings within the circuit.



a) Copper filled via

b) Coaxial via through core

c) Metal core exposed to allow removal of heat

Figure 6: Examples of metal-cored circuits

A more complex solution is metal-cored circuits. These can be usefully employed where space is limited and high isolation between RF and control is required in addition to thermal management. Heat being transferred from components to the core can either be through thermal vias or by direct contact through cavities within the circuit that the components are mounted on. Consideration must be given to removing heat from the core. Typically circuit substrate is machined away from two edges to expose the core so it may be clamped within the chassis to transfer heat. In the case of thermal vias where holes are blind with diameters <0.2mm and depths <0.3mm the holes can be filled with copper using a blind hole plating process. Figure 6 shows examples.

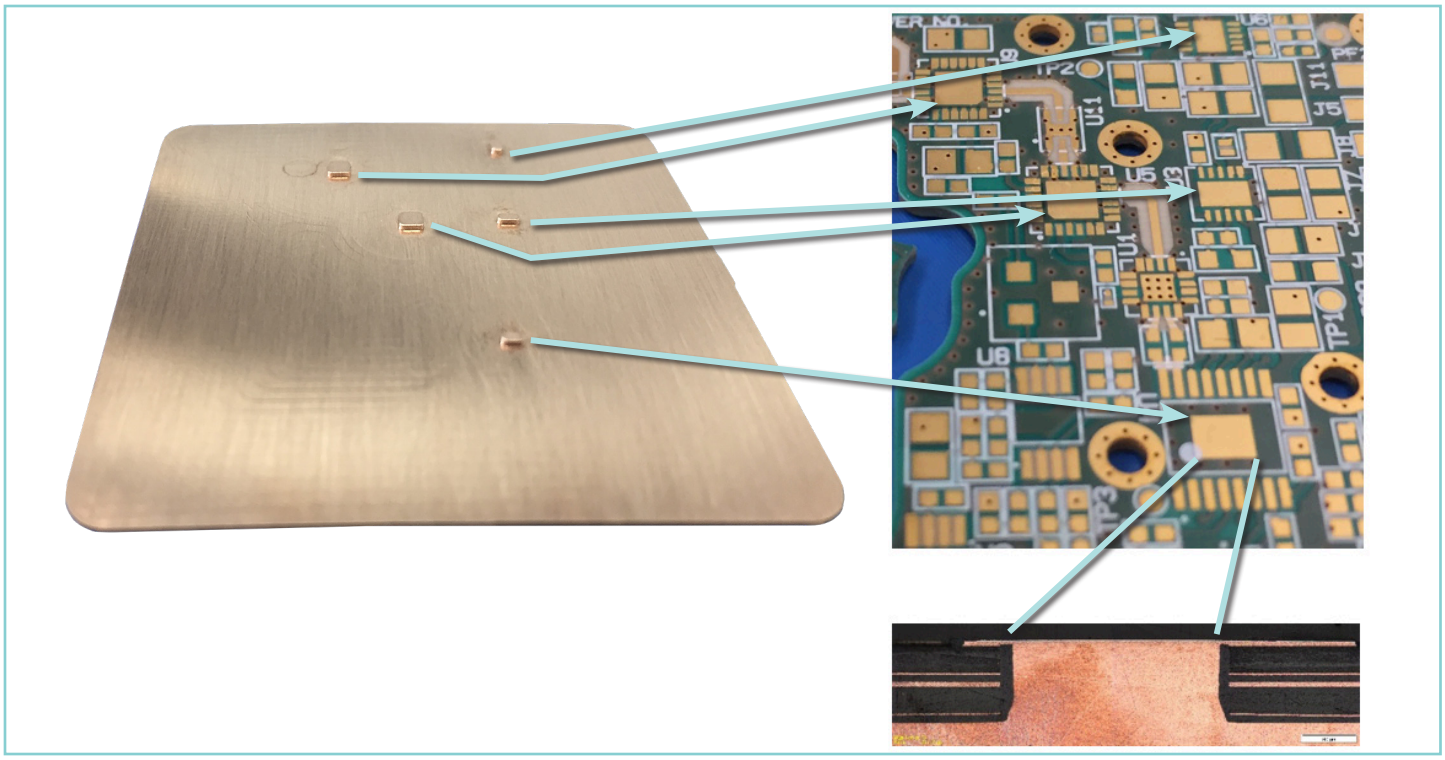


Figure 7: Machined copper plane with up-stands, applicable for small circuits

Another technique developed by Teledyne Labtech for thermal management on small circuits (<25cm^2) and where the overall thickness is limited, yet several devices require thermal management is to employ a machined copper plane with up-stands (pillars). This provides an excellent thermal path way and the heat can be distributed efficiently through the thermal plane for transmission to a cold wall. An example is shown in Figure 7.

Summary

For very high power applications, metal backed circuits currently offer the best solution for high power solid state RF devices that are flange mounted; they do not cater well for SMT components requiring thermal management. Where SMT components with high dissipation requirements are used, coins provide an effective solution for thermal management. If the required power dissipation is lower, thick walled filled vias offer a lower cost alternative to coins. Metal core and machined copper planes are generally only employed where space is limited and cost is not the overriding factor. There are thermally conductive substrates available for RF applications but even these generally have rather modest thermal conductivity of typically 1.0 to 1.5 W/mK

For More Information

If you require more information or have any enquiries regarding a specific application please email ptn_sales@teledyne.com or contact us via our website www.teledynedefelec.com.

Appendix 1 – Modelled PTHs

The following simplified calculations relate to Figure 2.

a) Thermal Vias assuming non-conductive filler

Drill @	0.500	
Plate through with	0.100	
Via Length	1.000	mm
Pitch	0.700	
Area for thermal vias	6.000	long
	6.000	wide
Number vias	64.000	
Total area of copper through vias	8.042	mm^2
Thermal conductivity of Cu	400	W/m.K
Non-conductive filler	0.6	W/m.K
Total area of epoxy in vias	4.524	
Thermal resistance copper Rth=L/kA	0.311	°C/W
Thermal resistance Epoxy Rth=L/kA	368.414	°C/W
Total Thermal resistance	**0.311**	°C/W
Total Thermal conductance	**3.220**	W/ °C

b) Thermal Vias assuming non-conductive filler

Drill @	0.300	
Plate through with	0.100	
Via Length	1.000	mm
Pitch	0.500	
Area for thermal vias	6.000	long
	6.000	wide
Number vias	144.000	
Total area of copper through vias	9.048	mm^2
Thermal conductivity of Cu	400	W/m.K
Non-conductive filler	0.6	W/m.K
Total area of epoxy in vias	1.131	
Thermal resistance copper Rth=L/kA	0.276	°C/W
Thermal resistance Epoxy Rth=L/kA	1473.657	°C/W
Total Thermal resistance	**0.276**	°C/W
Total Thermal conductance	**3.620**	W/ °C

c) Thermal Vias assuming conductive filler 4W/mK

Drill @	0.300	
Plate through with	0.100	
Via Length	1.000	mm
Pitch	0.500	
Area for thermal vias	6.000	long
	6.000	wide
Number vias	144.000	
Total area of copper through vias	9.048	mm^2
Thermal conductivity of Cu	400	W/m.K
Thermal filler Ag epoxy	4.0	W/m.K
Total area of Ag epoxy in vias	1.131	
Thermal resistance copper Rth=L/kA	0.276	°C/W
Thermal resistance Ag Epoxy Rth=L/kA	221.049	°C/W
Total Thermal resistance	**0.276**	°C/W
Total Thermal conductance	**3.624**	W/ °C

d) Thermal Vias assuming conductive filler 30W/mK

Drill @	0.300	
Plate through with	0.100	
Via Length	1.000	mm
Pitch	0.500	
Area for thermal vias	6.000	long
	6.000	wide
Number vias	144.000	
Total area of copper through vias	9.048	mm^2
Thermal conductivity of Cu	400	W/m.K
Thermal filler Ag epoxy	30.0	W/m.K
Total area of Ag epoxy in vias	1.131	
Thermal resistance copper Rth=L/kA	0.276	°C/W
Thermal resistance Ag Epoxy Rth=L/kA	29.473	o°C/W
Total Thermal resistance	**0.274**	°C/W
Total Thermal conductance	**3.653**	W/ °C

Appendix 2 – Modelled Copper Coins

The following simplified calculations relate to Figure 3.

a) Solid Copper Coin non-stepped

Dimensions of coin	6.000	long
	6.000	wide
Thickness of coin	1.000	mm
Total area of copper coin	36.000	mm^2
Thermal conductivity of Cu	400	W/m.K
Total Thermal resistance Rth=L/kA	**0.069**	°C/W
Total Thermal conductance	**14.400**	W/°C

b) Solid Copper Coin stepped

Dimensions of coin Top	6.000	long
	6.000	wide
Thickness of coin to step	0.300	mm
Area of copper coin Top	36.000	mm^2
Thermal resistance Top Rth=L/kA	**0.021**	°C/W
Dimensions of coin Base	8	long
	8	wide
Tickness of Base	0.7	mm
Area of copper coin Base	64.000	mm^2
Thermal resistance Base1 Rth=L/kA	**0.035**	°C/W
Thermal conductivity of Cu	400	W/m.K
Total Thermal resistance	0.056	°C/W
Total Thermal conductance	**17.910**	W/ °C

[1]Assumes only 50% of increased base area is efffective (50mm^2)