



# CY7C130/CY7C131 CY7C140/CY7C141

## 1K x 8 Dual-Port Static Ram

### Features

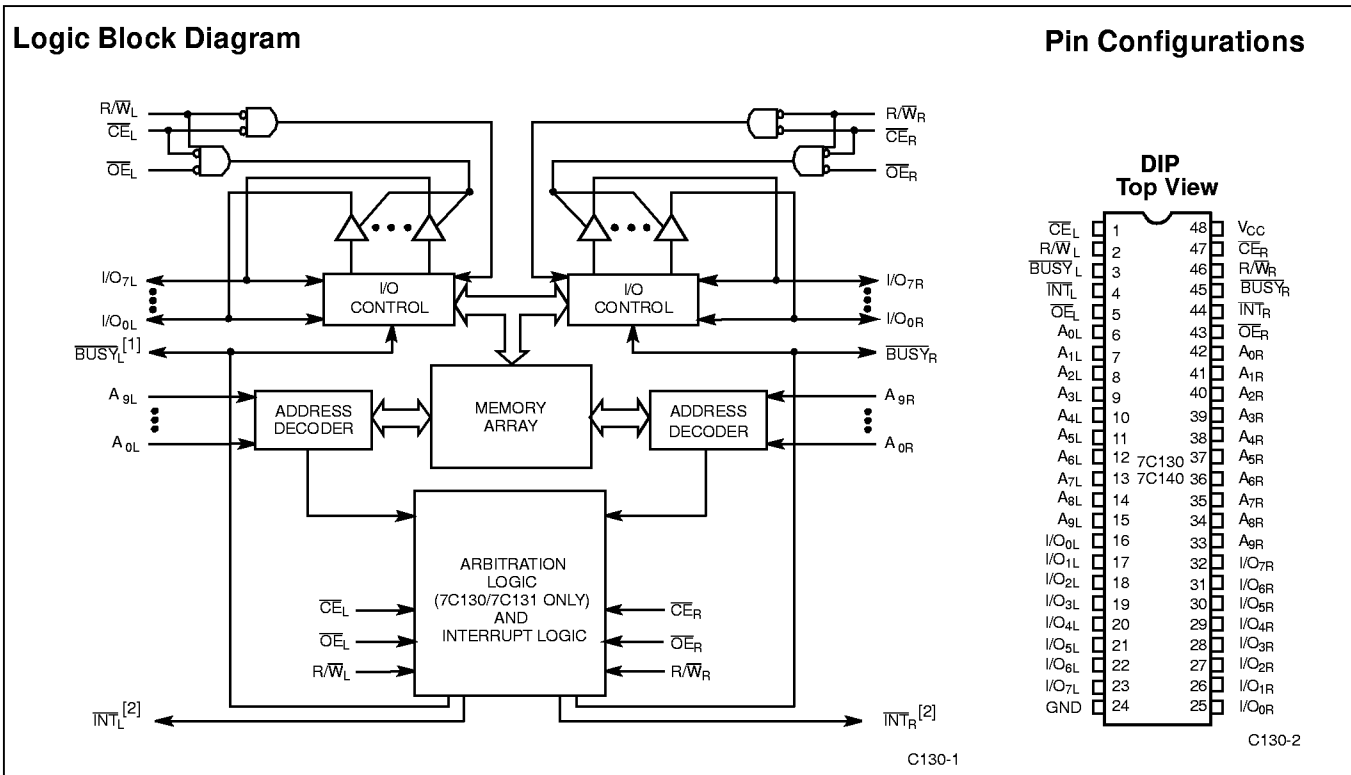
- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- 1K x 8 organization
- 0.65-micron CMOS for optimum speed/power
- High-speed access: 15 ns
- Low operating power:  $I_{CC} = 110 \text{ mA (max.)}$
- Fully asynchronous operation
- Automatic power-down
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141
- **BUSY** output flag on CY7C130/CY7C131; **BUSY** input on CY7C140/CY7C141
- **INT** flag for port-to-port communication
- Available in 48-pin DIP (CY7C130/140), 52-pin PLCC and 52-pin TQFP
- Pin-compatible and functionally equivalent to IDT7130/IDT7140

### Functional Description

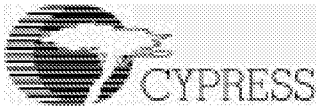
The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/ CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ( $\overline{CE}$ ), write enable ( $R/\overline{W}$ ), and output enable ( $\overline{OE}$ ). Two flags are provided on each port, **BUSY** and **INT**. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. **INT** is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ( $\overline{CE}$ ) pins.

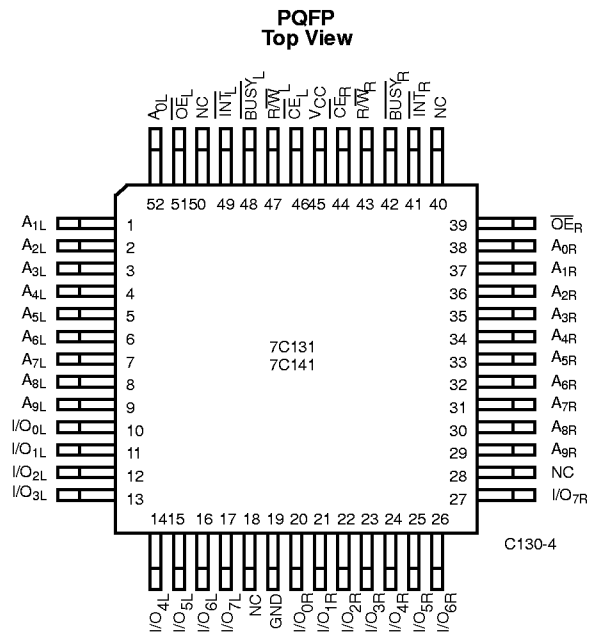
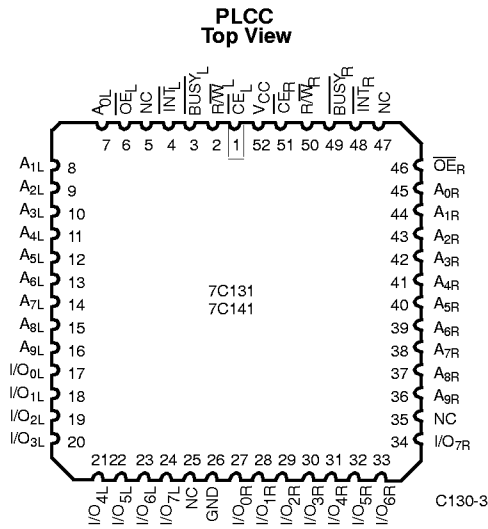
The CY7C130 and CY7C140 are available in 48-pin DIP. The CY7C131 and CY7C141 are available in 52-pin PLCC and PQFP.



- Notes:**
1. CY7C130/CY7C131 (Master): **BUSY** is open drain output and requires pull-up resistor  
CY7C140/CY7C141 (Slave): **BUSY** is input.
  2. Open drain outputs: pull-up resistor required



**Pin Configuration (continued)**



**Selection Guide**

		7C131-15 <sup>[3,4]</sup> 7C141-15	7C131-25 <sup>[3]</sup> 7C141-25	7C130-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		15	25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	190	170	170	120	120	110
	Military				170	170	120
Maximum Standby Current (mA)	Com'l/Ind	75	65	65	45	45	35
	Military				65	65	45

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

**Notes:**

- 3. 15 and 25-ns version available only in PLCC/PQFP packages.
- 4. Shaded area contains preliminary information.
- 5. T<sub>A</sub> is the "instant on" case temperature

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military <sup>[5]</sup>	-55°C to +125°C	5V ± 10%



Electrical Characteristics Over the Operating Range<sup>[6]</sup>

Parameter	Description	Test Conditions	7C131-15 <sup>[3,4]</sup> 7C141-15		7C130-30 <sup>[3]</sup> 7C131-25,30 7C140-30 7C141-25,30		7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 4.0 mA		0.4		0.4		0.4		0.4	V
		I <sub>OL</sub> = 16.0 mA <sup>[7]</sup>		0.5		0.5		0.5		0.5	
V <sub>IH</sub>	Input HIGH Voltage		2.2		2.2		2.2		2.2		V
V <sub>IL</sub>	Input LOW Voltage			0.8		0.8		0.8		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[8, 9]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	$\overline{CE} = V_{IL}$ , Outputs Open, f = f <sub>MAX</sub> <sup>[10]</sup>	Com'l	190		170		120		110	mA
			Mil					170		120	
I <sub>SB1</sub>	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , f = f <sub>MAX</sub> <sup>[10]</sup>	Com'l	75		65		45		35	mA
			Mil					65		45	
I <sub>SB2</sub>	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ , Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[10]</sup>	Com'l	135		115		90		75	mA
			Mil					115		90	
I <sub>SB3</sub>	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0	Com'l	15		15		15		15	mA
			Mil					15		15	
I <sub>SB4</sub>	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[10]</sup>	Com'l	125		105		85		70	mA
			Mil					105		85	

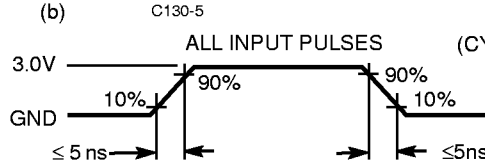
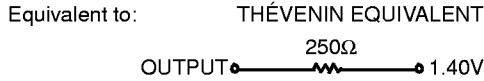
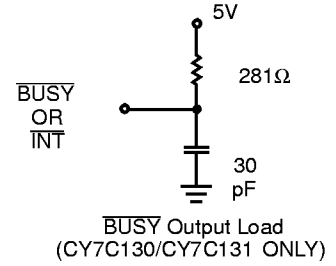
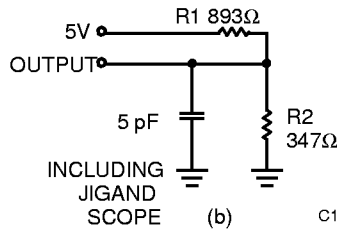
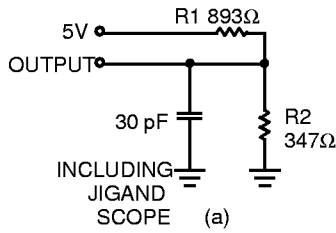
Notes:

6. See the last page of this specification for Group A subgroup testing information.
7. BUSY and INT pins only.
8. Duration of the short circuit should not exceed 30 seconds.
9. This parameter is guaranteed but not tested.
10. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>RC</sub> and using AC Test Waveforms input levels of GND to 3V.

Capacitance<sup>[9]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	15	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**AC Test Loads and Waveforms**

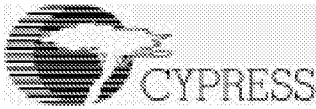


**Switching Characteristics** Over the Operating Range<sup>[6,11]</sup>

Parameter	Description	7C131-15 <sup>[3,4]</sup> 7C141-15		7C130-25 <sup>[3]</sup> 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE<sup>[15]</sup></b>								
t <sub>RC</sub>	Read Cycle Time	15		25		30		ns
t <sub>AA</sub>	Address to Data Valid <sup>[12]</sup>		15		25		30	ns
t <sub>OHA</sub>	Data Hold from Address Change	0		0		0		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid <sup>[12]</sup>		15		25		30	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid <sup>[12]</sup>		10		15		20	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[9,13,14]</sup>	3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[9,13,14]</sup>		10		15		15	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[9,13,14]</sup>	3		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[9,13,14]</sup>		10		15		15	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up <sup>[9]</sup>	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down <sup>[9]</sup>		15		25		25	ns
<b>WRITE CYCLE<sup>[15]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	15		25		30		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	12		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	12		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	2		2		2		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	R/W Pulse Width	12		15		25		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	R/W LOW to High Z <sup>[14]</sup>		10		15		15	ns
t <sub>LZWE</sub>	R/W HIGH to Low Z <sup>[14]</sup>	0		0		0		ns

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- AC Test Conditions use V<sub>OH</sub> = 1.6V and V<sub>OL</sub> = 1.4V.
- At any given temperature and voltage condition for any given device, t<sub>HZOE</sub> is less than t<sub>LZOE</sub> and t<sub>HZCE</sub> is less than t<sub>LZCE</sub>.
- t<sub>LZOE</sub>, t<sub>LZWE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>HZOE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and R/W LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



**Switching Characteristics** Over the Operating Range<sup>[6,11]</sup> (continued)

Parameter	Description	7C131-15 <sup>[3,4]</sup> 7C141-15		7C130-25 <sup>[3]</sup> 7C131-25 7C140-25 7C141-25		7C130-30 7C131-30 7C140-30 7C141-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUSY/INTERRUPT TIMING</b>								
t <sub>BLA</sub>	BUSY LOW from Address Match		15		20		20	ns
t <sub>BHA</sub>	BUSY HIGH from Address Mismatch <sup>[16]</sup>		15		20		20	ns
t <sub>BLC</sub>	BUSY LOW from $\overline{CE}$ LOW		15		20		20	ns
t <sub>BHC</sub>	BUSY HIGH from $\overline{CE}$ HIGH <sup>[16]</sup>		15		20		20	ns
t <sub>PS</sub>	Port Set Up for Priority	5		5		5		ns
t <sub>WB</sub> <sup>[17]</sup>	R/W LOW after BUSY LOW	0		0		0		ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH	13		20		30		ns
t <sub>BDD</sub>	BUSY HIGH to Valid Data		15		25		30	ns
t <sub>DDD</sub>	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18	ns
t <sub>WDD</sub>	Write Pulse to Data Delay		Note 18		Note 18		Note 18	ns
<b>INTERRUPT TIMING</b>								
t <sub>WINS</sub>	R/W to INTERRUPT Set Time		15		25		25	ns
t <sub>EINS</sub>	$\overline{CE}$ to INTERRUPT Set Time		15		25		25	ns
t <sub>INS</sub>	Address to INTERRUPT Set Time		15		25		25	ns
t <sub>OINR</sub>	$\overline{OE}$ to INTERRUPT Reset Time <sup>[16]</sup>		15		25		25	ns
t <sub>EINR</sub>	$\overline{CE}$ to INTERRUPT Reset Time <sup>[16]</sup>		15		25		25	ns
t <sub>INR</sub>	Address to INTERRUPT Reset Time <sup>[16]</sup>		15		25		25	ns

**Notes:**

- 16. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
- 17. CY7C140/CY7C141 only.
- 18. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:  
 BUSY on Port B goes HIGH.  
 Port B's address is toggled.  
 $\overline{CE}$  for Port B is toggled.  
 R/W for Port B is toggled during valid read.

**Switching Characteristics** Over the Operating Range<sup>[6,11]</sup>

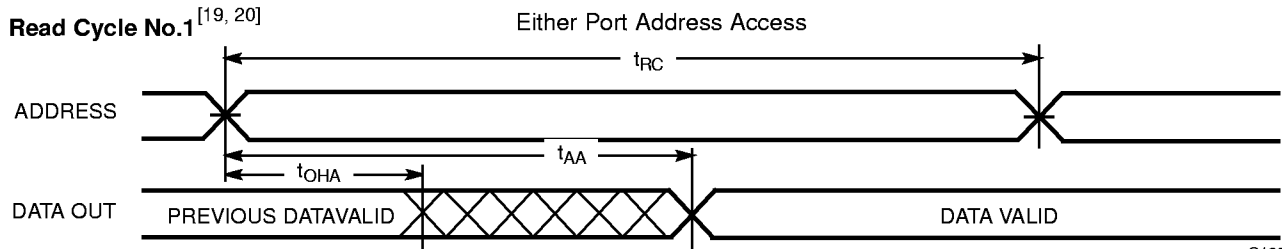
Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	35		45		55		ns
t <sub>AA</sub>	Address to Data Valid <sup>[12]</sup>		35		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	0		0		0		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid <sup>[12]</sup>		35		45		55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid <sup>[12]</sup>		20		25		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[9,13, 14]</sup>	3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[9,13, 14]</sup>		20		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[9,13, 14]</sup>	5		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[9,13, 14]</sup>		20		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up <sup>[9]</sup>	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down <sup>[9]</sup>		35		35		35	ns



Switching Characteristics Over the Operating Range<sup>[6,11]</sup> (continued)

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE<sup>[15]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	35		45		55		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	30		35		40		ns
t <sub>AW</sub>	Address Set-Up to Write End	30		35		40		ns
t <sub>HA</sub>	Address Hold from Write End	2		2		2		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	R/W Pulse Width	25		30		30		ns
t <sub>SD</sub>	Data Set-Up to Write End	15		20		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	R/W LOW to High Z <sup>[14]</sup>		20		20		25	ns
t <sub>LZWE</sub>	R/W HIGH to Low Z <sup>[14]</sup>	0		0		0		ns
<b>BUSY/INTERRUPT TIMING</b>								
t <sub>BLA</sub>	BUSY LOW from Address Match		20		25		30	ns
t <sub>BHA</sub>	BUSY HIGH from Address Mismatch <sup>[16]</sup>		20		25		30	ns
t <sub>BLC</sub>	BUSY LOW from $\overline{CE}$ LOW		20		25		30	ns
t <sub>BHC</sub>	BUSY HIGH from $\overline{CE}$ HIGH <sup>[16]</sup>		20		25		30	ns
t <sub>PS</sub>	Port Set Up for Priority	5		5		5		ns
t <sub>WB</sub> <sup>[17]</sup>	R/W LOW after BUSY LOW	0		0		0		ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH	30		35		35		ns
t <sub>BDD</sub>	BUSY HIGH to Valid Data		35		45		45	ns
t <sub>DDD</sub>	Write Data Valid to Read Data Valid		Note 18		Note 18		Note 18	ns
t <sub>WDD</sub>	Write Pulse to Data Delay		Note 18		Note 18		Note 18	ns
<b>INTERRUPT TIMING</b>								
t <sub>WINS</sub>	R/W to INTERRUPT Set Time		25		35		45	ns
t <sub>EINS</sub>	$\overline{CE}$ to INTERRUPT Set Time		25		35		45	ns
t <sub>INS</sub>	Address to INTERRUPT Set Time		25		35		45	ns
t <sub>OINR</sub>	$\overline{OE}$ to INTERRUPT Reset Time <sup>[16]</sup>		25		35		45	ns
t <sub>EINR</sub>	$\overline{CE}$ to INTERRUPT Reset Time <sup>[16]</sup>		25		35		45	ns
t <sub>INR</sub>	Address to INTERRUPT Reset Time <sup>[16]</sup>		25		35		45	ns

Switching Waveforms



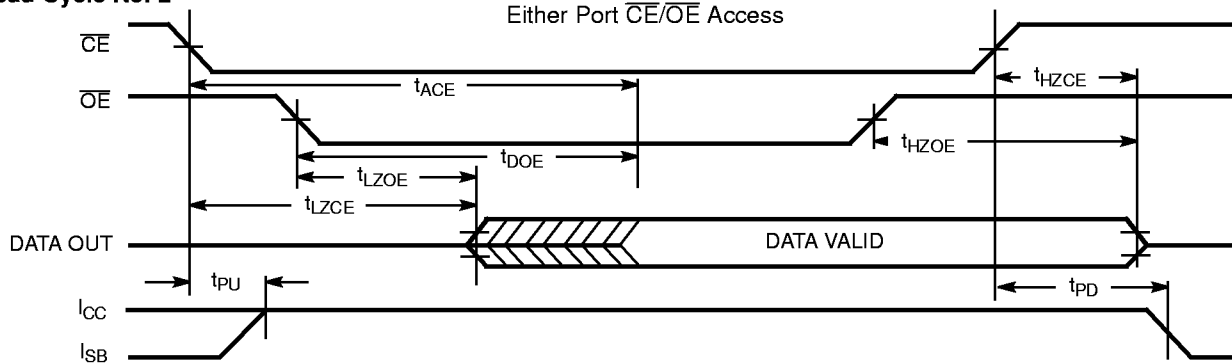
C130-7

Notes:

- 19. R/W is HIGH for read cycle.
- 20. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .

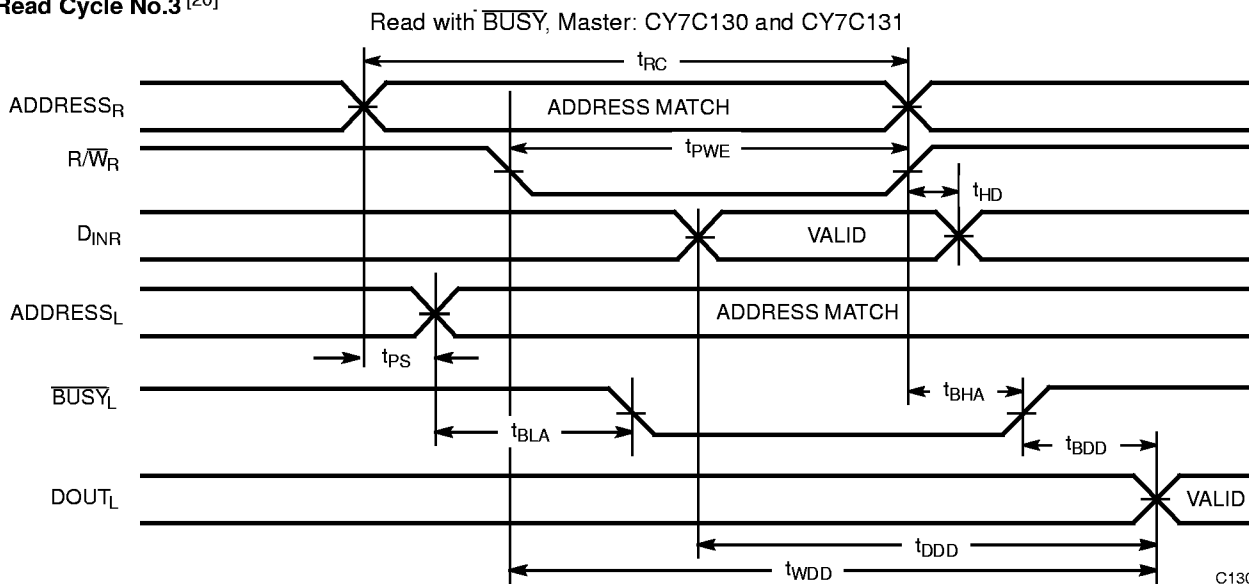
**Switching Waveforms** (continued)

**Read Cycle No. 2** [19, 21]



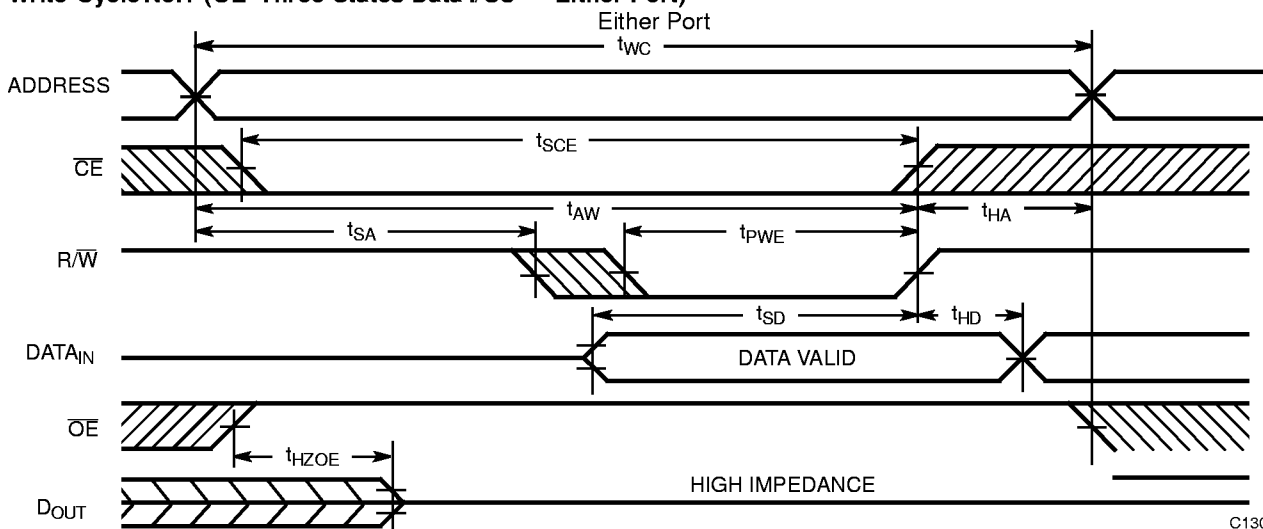
C130-8

**Read Cycle No. 3** [20]



C130-9

**Write Cycle No. 1 (OE Three-States Data I/Os - Either Port)** [15, 22]



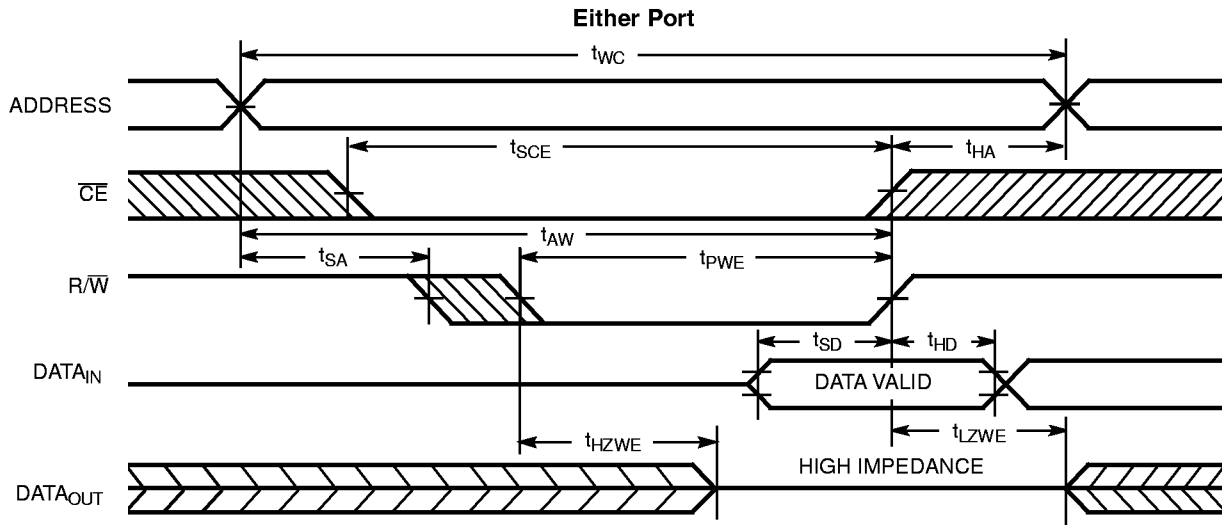
C130-10

**Notes:**

21. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
22. If  $\overline{OE}$  is LOW during a R/ $\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $t_{HZWE} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .

Switching Waveforms (continued)

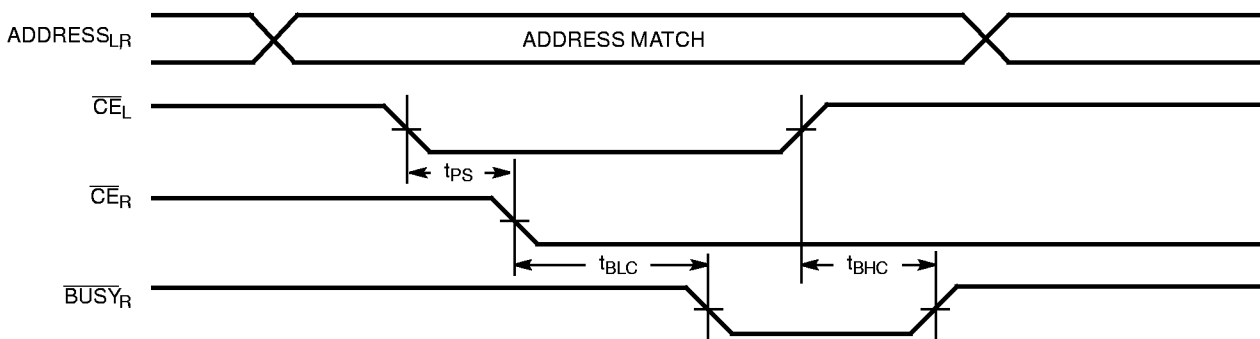
Write Cycle No. 2 (R/W Three-States Data I/Os - Either Port) <sup>[16, 23]</sup>



C130-11

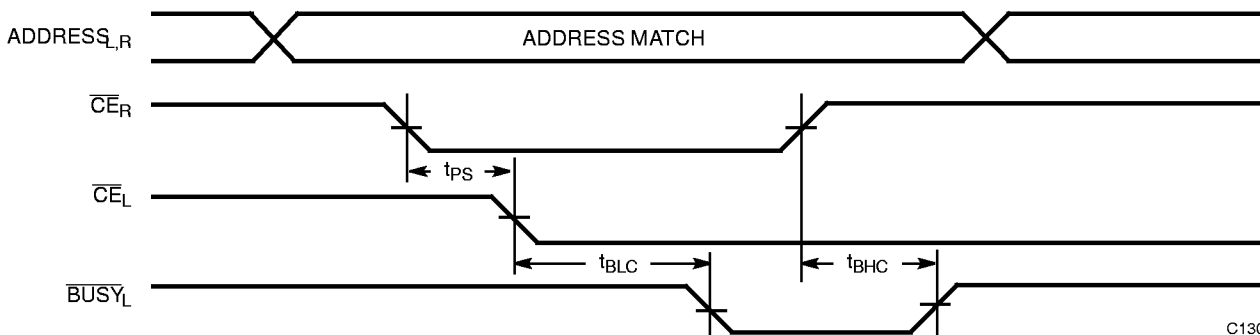
Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)

$\overline{CE}_L$  Valid First:



C130-12

$\overline{CE}_R$  Valid First:



C130-13

Note:

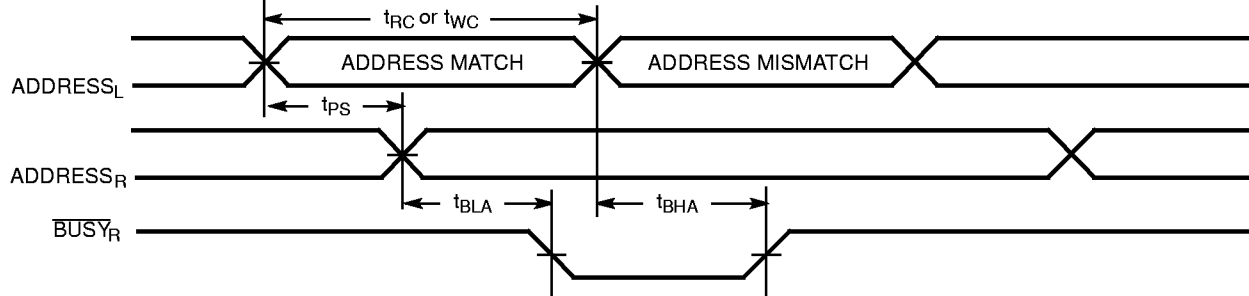
23. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state



Switching Waveforms (continued)

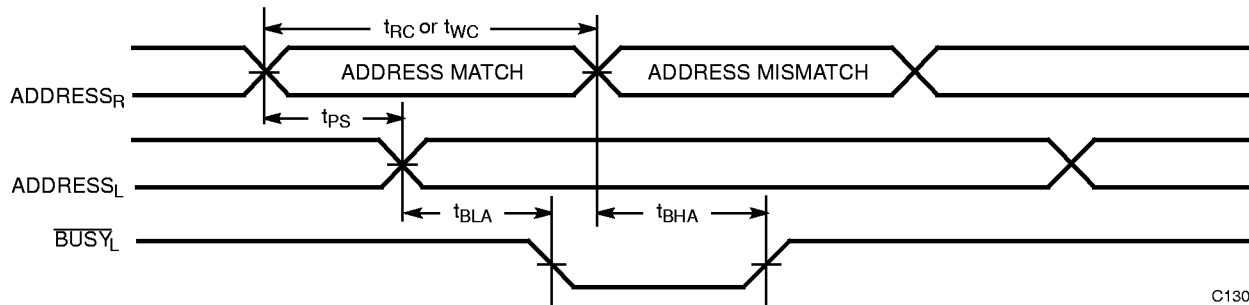
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



C130-14

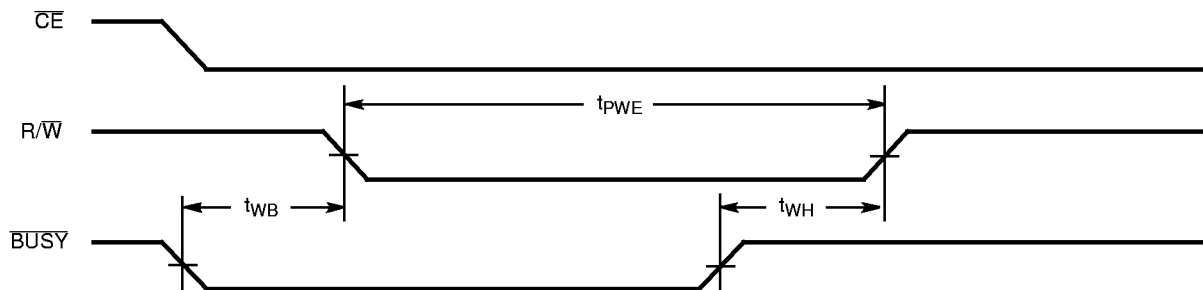
Right Address Valid First:



C130-15

Busy Timing Diagram No. 3

Write with  $\overline{\text{BUSY}}$  (Slave:CY7C140/CY7C141)

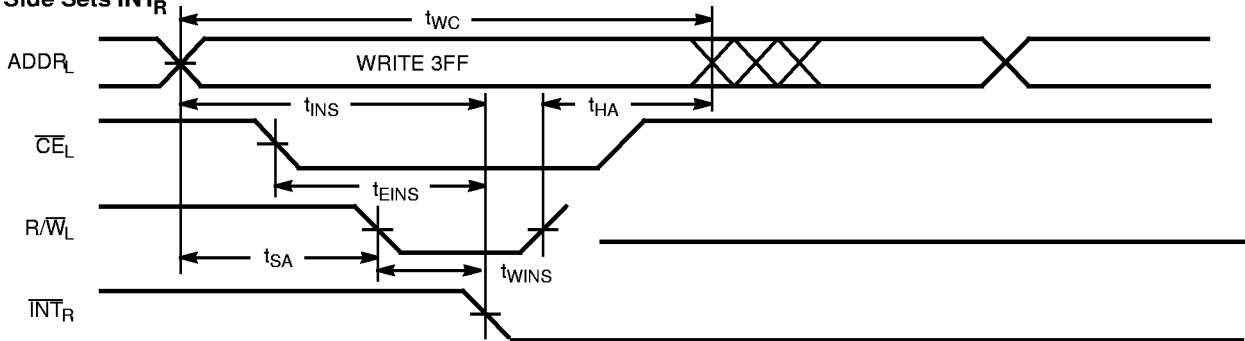


C130-16

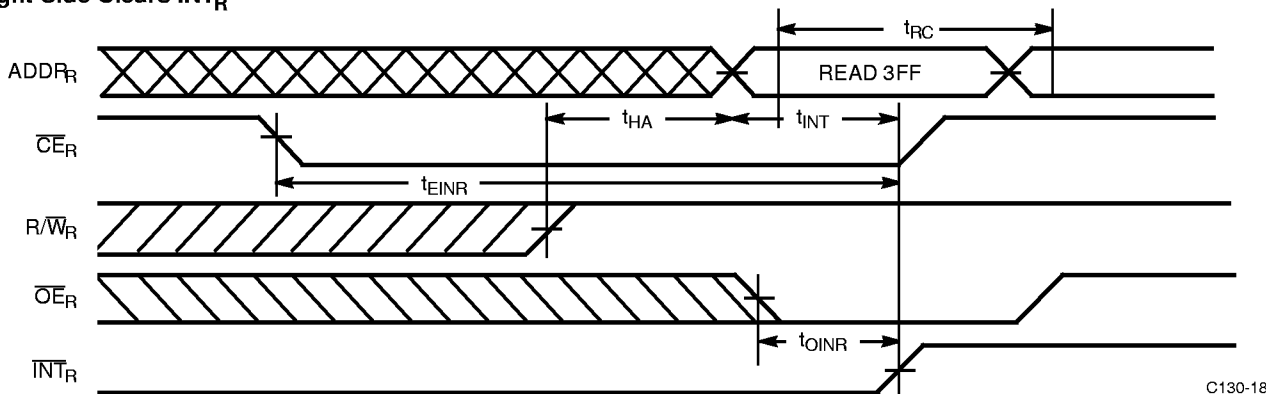
Switching Waveforms (continued)

Interrupt Timing Diagrams

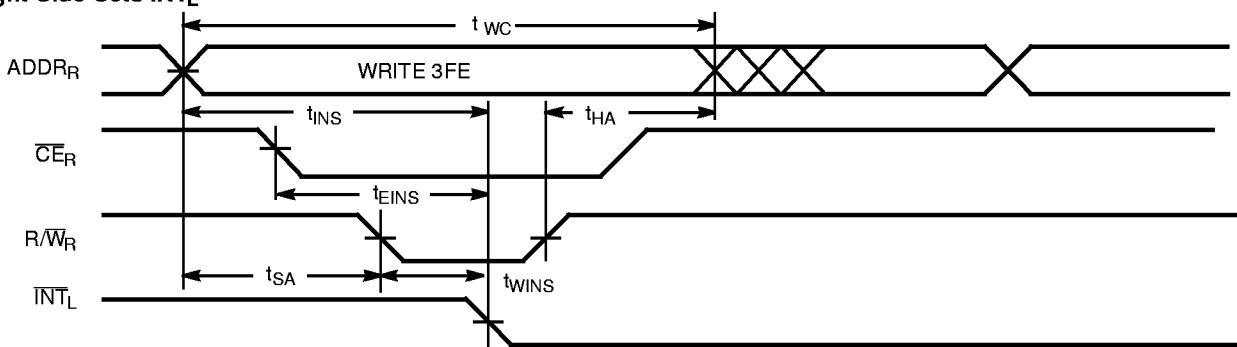
Left Side Sets  $\overline{INT}_R$



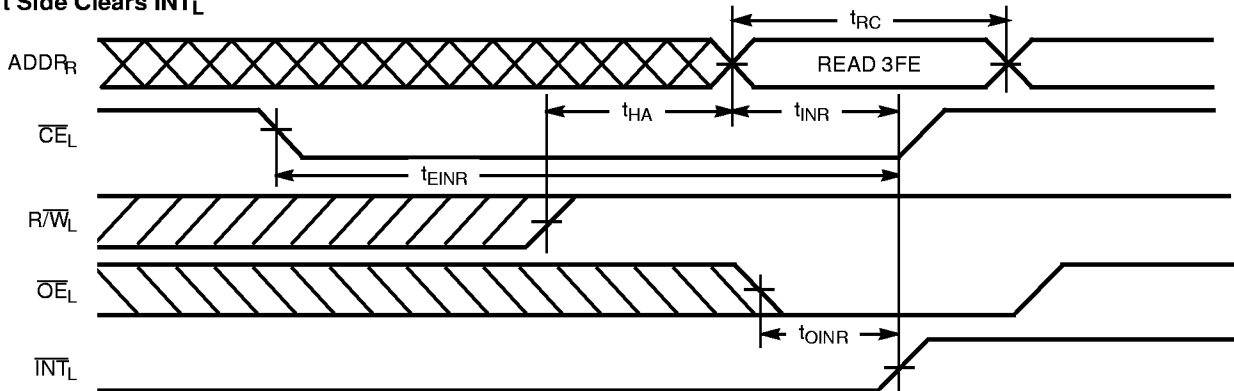
Right Side Clears  $\overline{INT}_R$

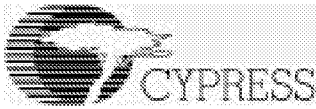


Right Side Sets  $\overline{INT}_L$

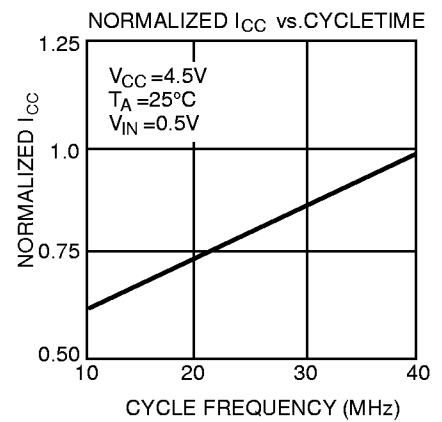
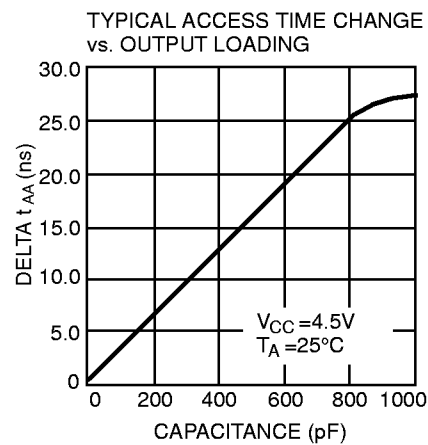
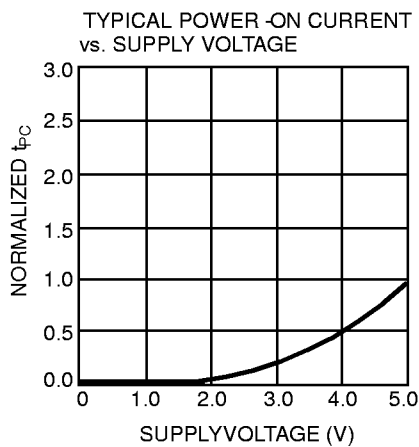
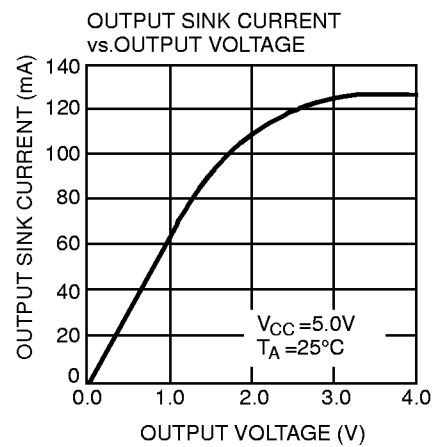
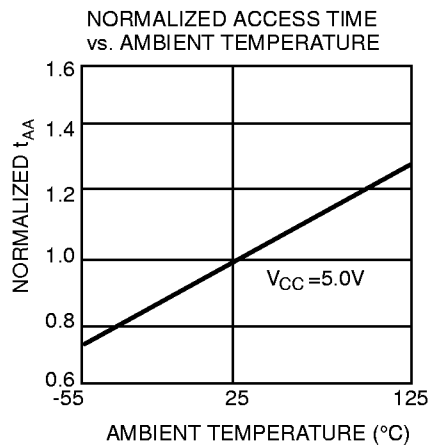
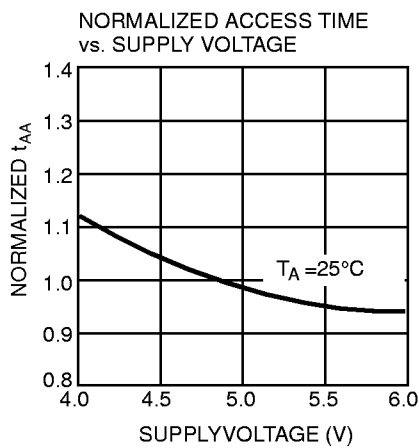
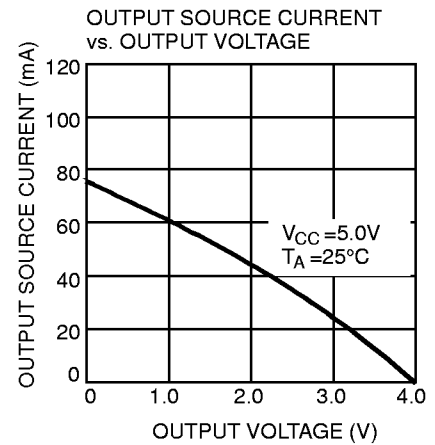
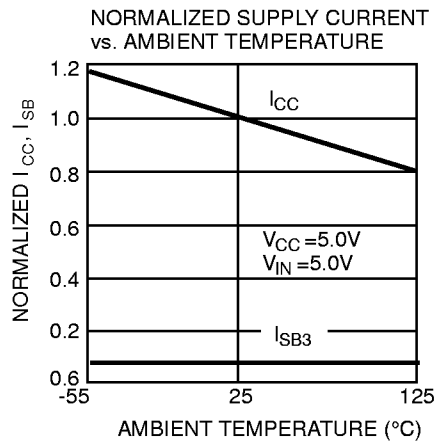
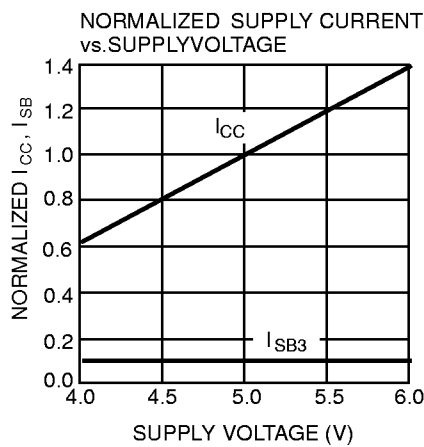


Left Side Clears  $\overline{INT}_L$





Typical DC and AC Characteristics





**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C130-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C130-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C131-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C131-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C131-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C131-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131-55NI	N52	52-Pin Plastic Quad Flatpack	

Shaded area contains preliminary information.



**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C140-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C140-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C141-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C141-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-35NI	N52	52-Pin Plastic Quad Flatpack	
45	CY7C141-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-45NI	N52	52-Pin Plastic Quad Flatpack	
55	CY7C141-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141-55NI	N52	52-Pin Plastic Quad Flatpack	

Shaded area contains preliminary information.



**MILITARY SPECIFICATIONS**

**Group A Subgroup Testing**

**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub> Max.	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3
I <sub>SB3</sub>	1, 2, 3
I <sub>SB4</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
READ CYCLE	
t <sub>RC</sub>	7, 8, 9, 10, 11
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>ACE</sub>	7, 8, 9, 10, 11
t <sub>DOE</sub>	7, 8, 9, 10, 11
WRITE CYCLE	
t <sub>WC</sub>	7, 8, 9, 10, 11
t <sub>SCE</sub>	7, 8, 9, 10, 11
t <sub>AW</sub>	7, 8, 9, 10, 11
t <sub>HA</sub>	7, 8, 9, 10, 11
t <sub>SA</sub>	7, 8, 9, 10, 11
t <sub>PWE</sub>	7, 8, 9, 10, 11
t <sub>SD</sub>	7, 8, 9, 10, 11
t <sub>HD</sub>	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t <sub>BLA</sub>	7, 8, 9, 10, 11
t <sub>BHA</sub>	7, 8, 9, 10, 11
t <sub>BLC</sub>	7, 8, 9, 10, 11
t <sub>BHC</sub>	7, 8, 9, 10, 11
t <sub>PS</sub>	7, 8, 9, 10, 11
t <sub>WINS</sub>	7, 8, 9, 10, 11
t <sub>EINS</sub>	7, 8, 9, 10, 11
t <sub>INS</sub>	7, 8, 9, 10, 11
t <sub>OINR</sub>	7, 8, 9, 10, 11
t <sub>EINR</sub>	7, 8, 9, 10, 11
t <sub>INR</sub>	7, 8, 9, 10, 11
BUSY TIMING	
t <sub>WB</sub> <sup>[24]</sup>	7, 8, 9, 10, 11
t <sub>WH</sub>	7, 8, 9, 10, 11
t <sub>BDD</sub>	7, 8, 9, 10, 11

**Note:**

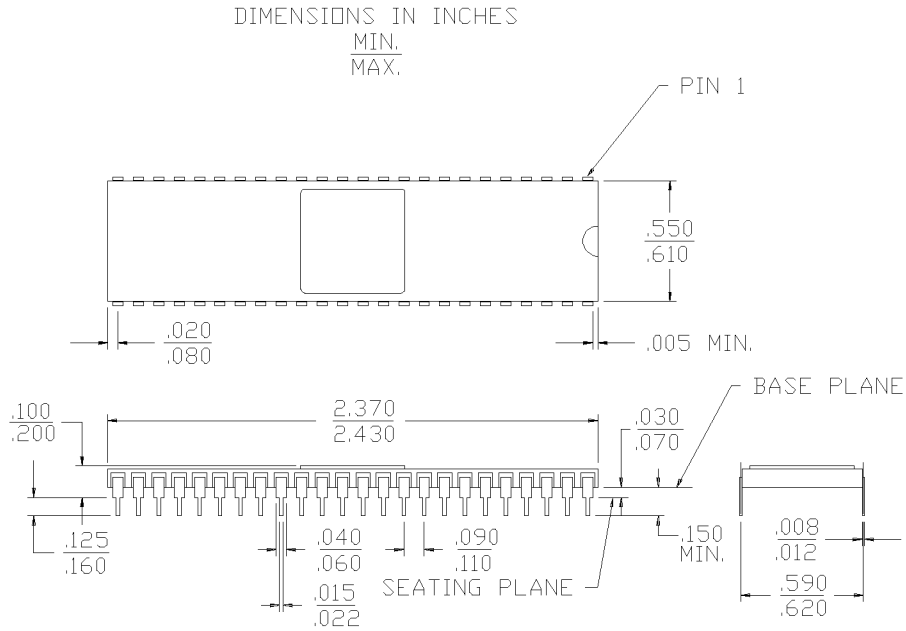
24. CY7C140/CY7C141 only.

Document #: 38-00027-M

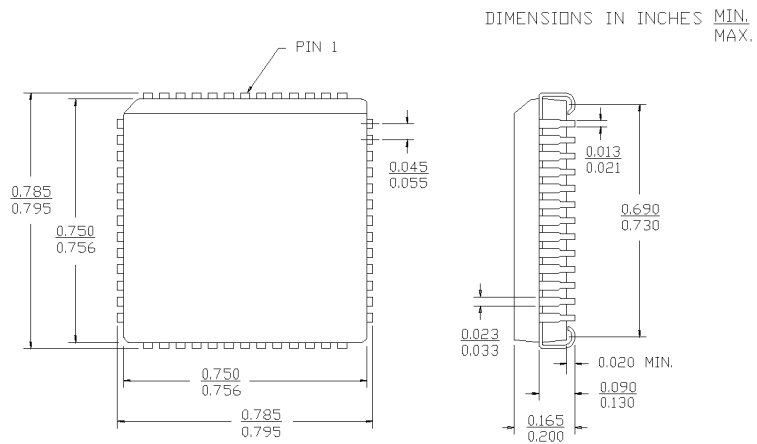
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**Package Diagrams**

**48-Lead (600-Mil) Sidebrazed DIP D26**



**52-Lead Plastic Leaded Chip Carrier J69**





Package Diagrams (continued)

48-Lead (600-Mil) Molded DIP P25

