

Improving Phase Noise of PLLs at Low Frequencies

Introduction

Peregrine Semiconductor's integer-N and fractional-N PLL frequency synthesizers deliver superior phase noise performance where ultra-low phase noise is critical. However, as the edge rate of the RF input signal decreases, the phase noise will begin to degrade. At this point, the best performance for phase noise is obtained for signals with a higher slew rate, such as a square wave.

This application note describes the prescaler bypass mode for low frequency operation and presents a method to improve the phase noise. This application note focuses on the PE97240 integer-N phase locked loop (PLL) frequency synthesizer, but can be applied to all Peregrine Semiconductor PLL products.

Summary

- Prescaler bypass mode supports low frequency operation.
- Phase noise will degrade as the slew rate RF input signal decreases below the minimum value.
- The RF input frequency may be decreased while maintaining the minimum slew rate.

The operating frequency of the PE97240 in prescaler bypass mode is 50 MHz to 800 MHz. Prescaler bypass mode can handle a slower slew rate and is recommended for lower VCO frequencies to realize the same phase noise as compared to normal operating mode. However, as the frequency decreases, it becomes difficult to keep up with minimum edge rate required using a sine wave. As the slew rate of the input signal decreases, at some point the phase noise will start to degrade. For example, a slew rate of 4 V/ns at 325 MHz is equivalent to a sine wave with amplitude of 2 V_{PK}. This level would exceed the maximum input power specification of the main divider. In order to maintain good phase noise performance, it is necessary to increase the edge rate of the RF input signal.

Application Example

Figure 2 shows a possible solution for a clock cleaning application where a PLL may be used to recover a noisy clock. In this example, the VCO supplies a low noise 100 MHz sine wave to the RF input of the PLL.

Figure 2. Block Diagram of 100 MHz PLL Test Circuit

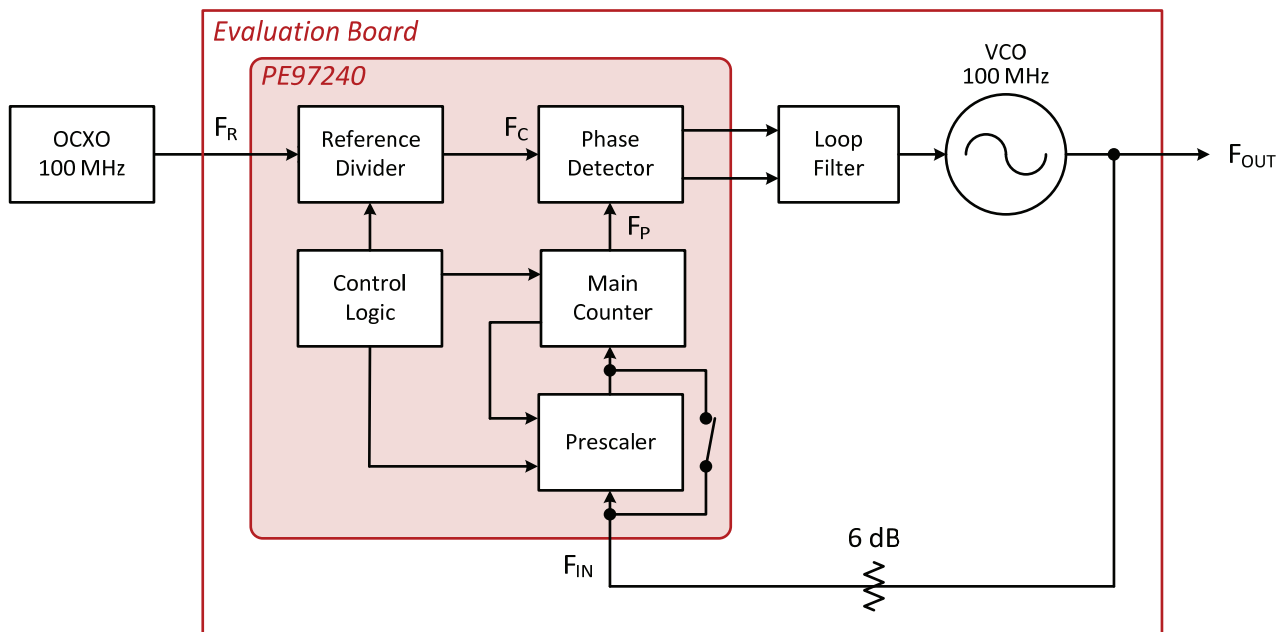
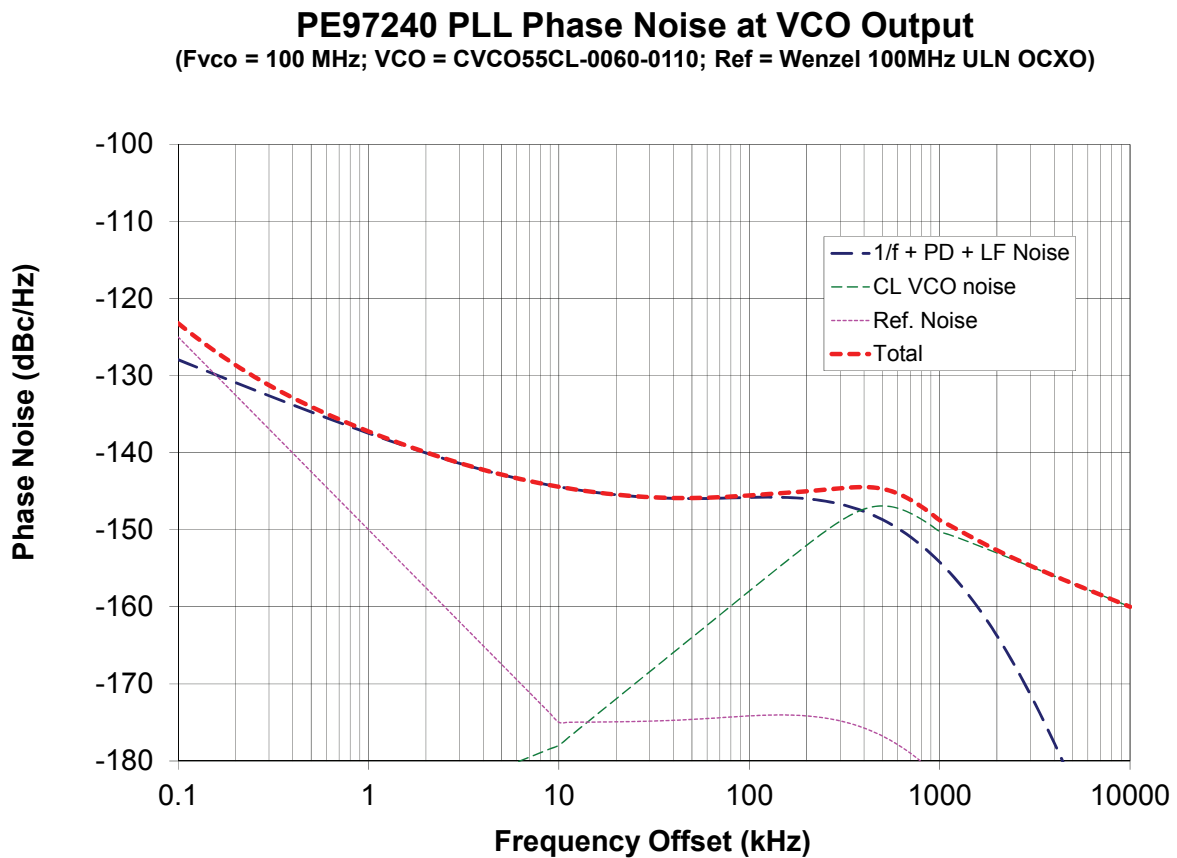


Figure 3 shows the simulated phase noise performance using the PE97240 PLL loop filter calculator and phase noise estimator spreadsheet*. In this example, the reference frequency (F_R) is 100 MHz, the comparison frequency (F_C) is 50 MHz and the loop bandwidth is 500 kHz. The loop bandwidth is extended in order to determine the normalized phase noise. Measuring the phase noise with a wider loop bandwidth more accurately captures the PLL.

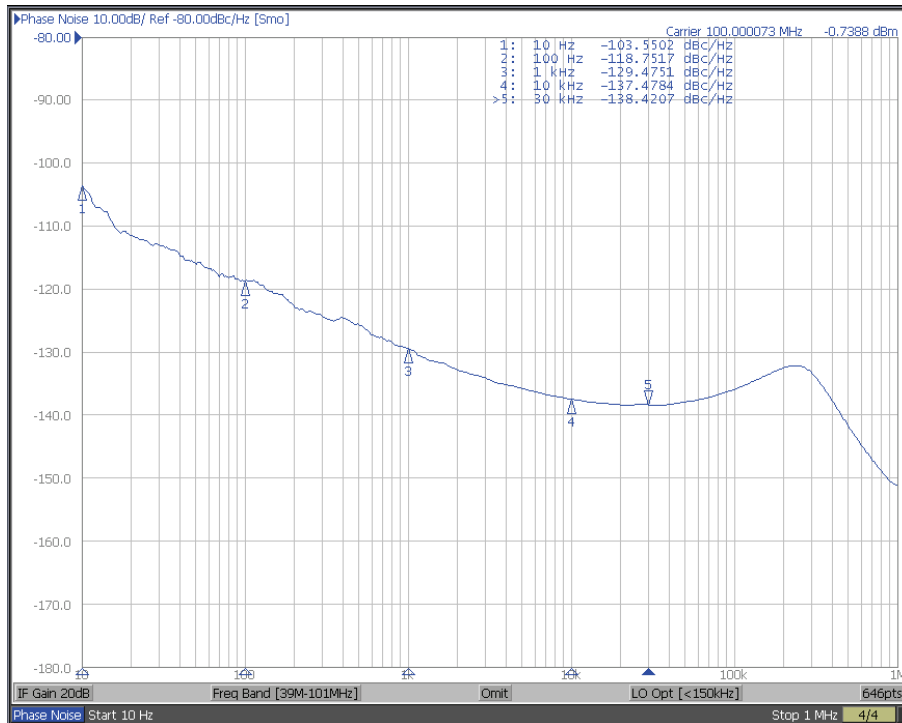
Note: * The phase detector PLL loop filter calculator and phase noise estimator spreadsheet can be downloaded at www.psemi.com.

Figure 3. Simulated Phase Noise Performance of the PE97420 at 100 MHz



From the estimated phase noise results, we would expect to achieve a normalized phase noise floor of -228 dBc/Hz. However, due to the slower edge rate of the 100 MHz sine wave, the actual measurement falls short of the expectation by achieving only -221 dBc/Hz as measured in *Figure 4*. Note that the VCO is the major wideband phase noise contributor and requires low phase noise.

Figure 4. Measured Phase Noise Performance Using a 100 MHz VCO with Sine Wave Output



To overcome the degraded phase noise performance, a low noise buffer is inserted at the VCO output as shown in *Figure 5*. The intent of the buffer is to increase the slew rate of the 100 MHz sine wave with minimal additive noise. The buffer used in this example is the LTC6957 from Linear Technology*. The LTC6957 is a very low phase noise, dual output AC signal bugger/driver/logic level translator. The LTC6957-4 option provides CMOS logic, complementary outputs and is available in a demo board.

Note: *The LTC6957 is used for demonstration purposes only and is not recommended for space-qualified applications.

To overcome the degraded phase noise performance, a low noise buffer is inserted at the VCO output as shown in *Figure 5*. The intent of the buffer is to increase the slew rate of the 100 MHz sine wave with minimal additive noise. The buffer used in this example is the LTC6957 from Linear Technology*. The LTC6957 is a very low phase noise, dual output AC signal bugger/driver/logic level translator. The LTC6957-4 option provides CMOS logic, complementary outputs and is available in a demo board.

Note: * The LTC6957 is used for demonstration purposes only and is not recommended for space-qualified applications.

Figure 5. Block Diagram of 100 MHz Test Circuit Showing VCO Buffered Output

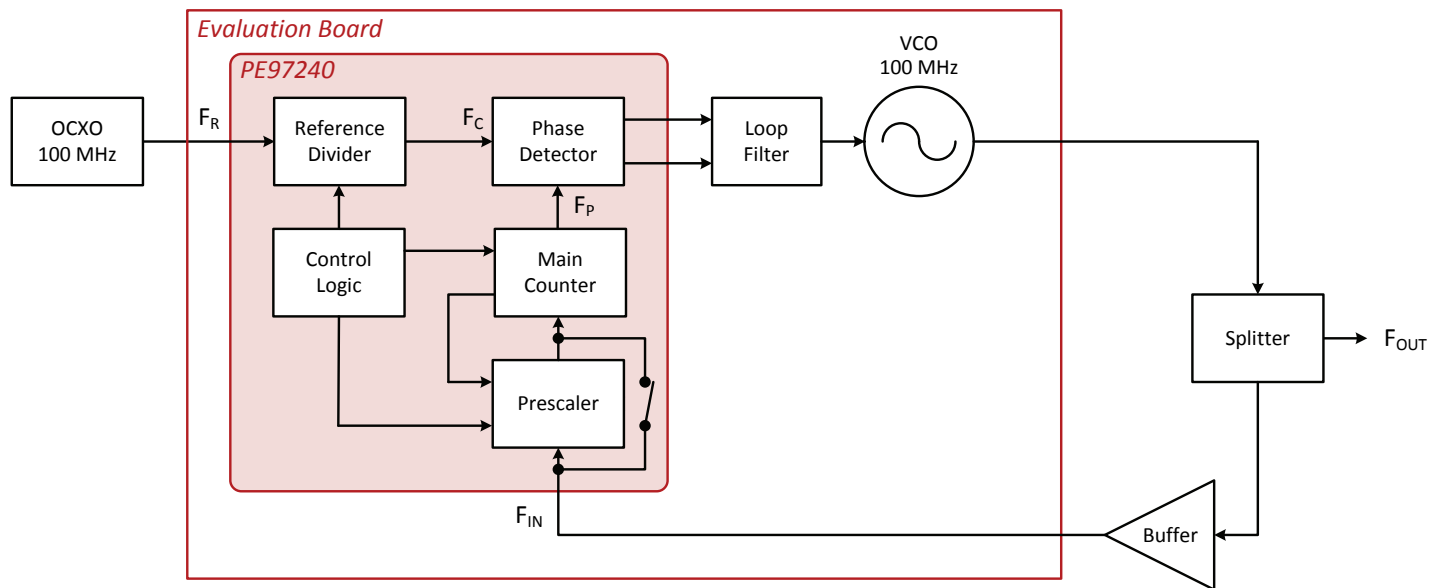
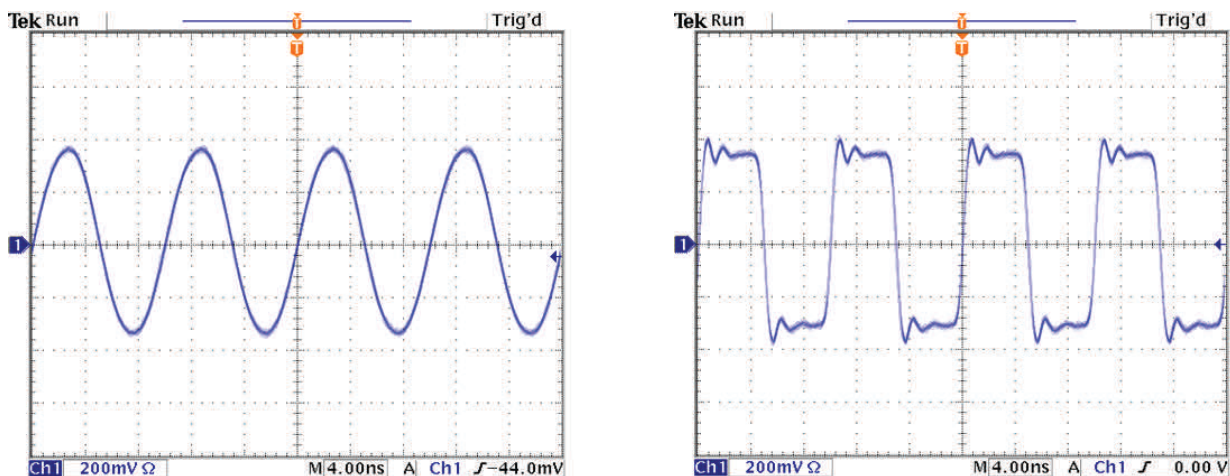


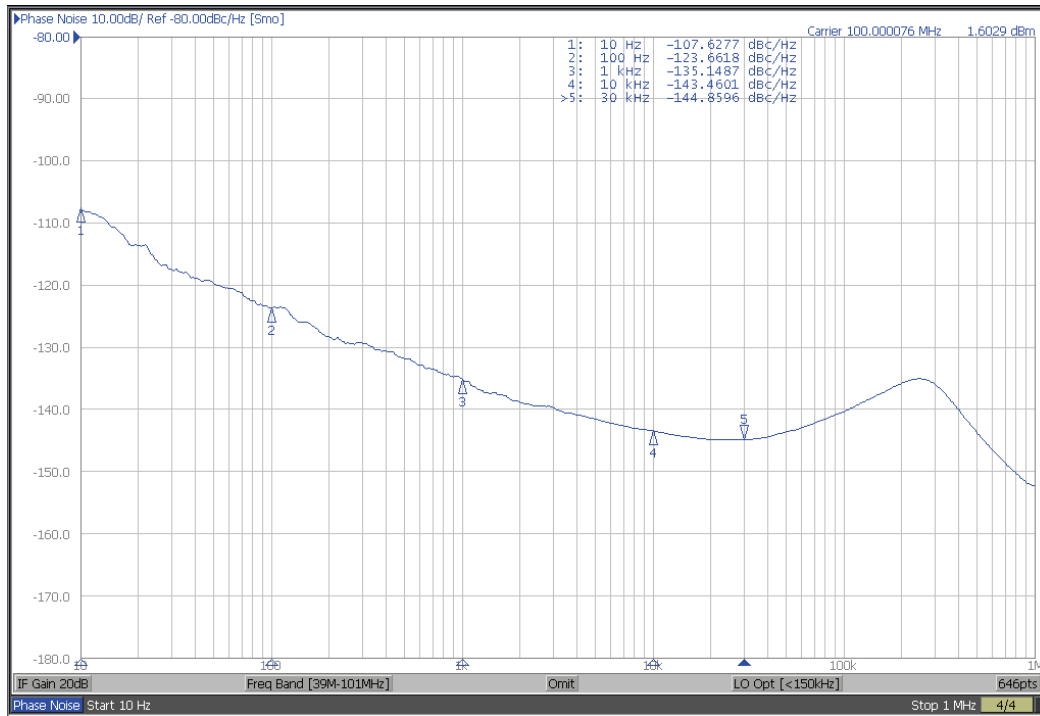
Figure 6 demonstrates the measured performance of the LTC6957-4 with a 100 MHz input sine wave and the resulting buffered output with faster edge rates.

Figure 6. LTC6957-4 Waveforms Showing a) 100 MHz Sine Wave Output and b) Buffered Output



The measured phase noise results in *Figure 7* indicate that the LTC6957-4 provides sufficient slew rate to the F_{IN} input. Additionally, the low additive phase noise of the LTC6957-4 has minimal impact on the PE97240 phase noise performance.

Figure 7. Measured Phase Noise Performance Using a 100 MHz VCO with a Buffered Output



Test Circuit Description

The simplified schematic of the PE97240 PLL with the LTC6957-4 demo board supplying the buffered VCO output is illustrated in *Figure 8*. An ultra-low noise OCXO is used as the reference source to ensure that the reference noise does not limit the phase noise measurements. The loop filter component values were determined from the PLL loop filter calculator and phase noise estimator spreadsheet as previously mentioned. The VCO with decent phase noise performance is readily available off the shelf. However, there is some wide band noise associated with the peaking response in the phase noise measurements. The power splitter and buffer are external to the PE97240 evaluation board. Note that it is also possible for the buffer to drive the RF input ports of the PE97240 differentially.

Figure 8. Simplified Schematic of PE97240 100 MHz Test Circuit with a Buffered VCO Output

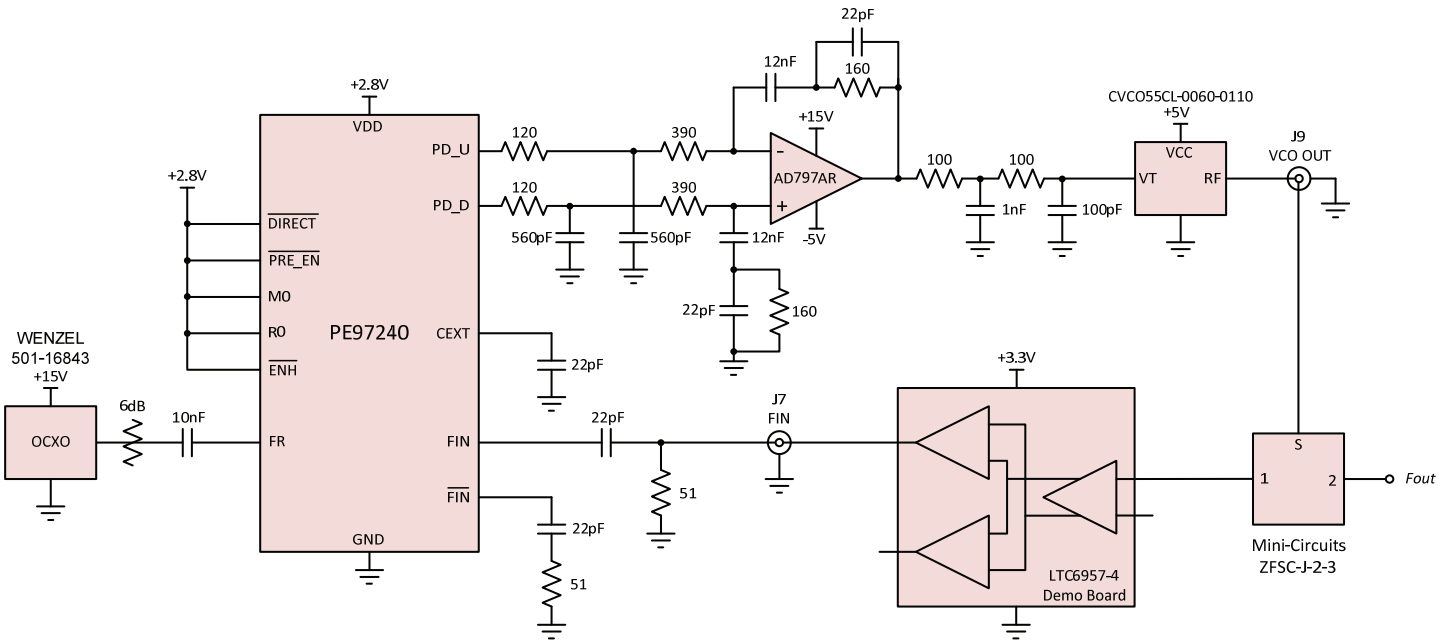


Figure 9 shows both the phase noise plots and the improvement obtained by improving the RF input slew rate with the buffer. The comparative normalized phase noise results are shown in Table 1.

Figure 9. Combined Phase Noise Plot Showing Improved Performance at 100 MHz

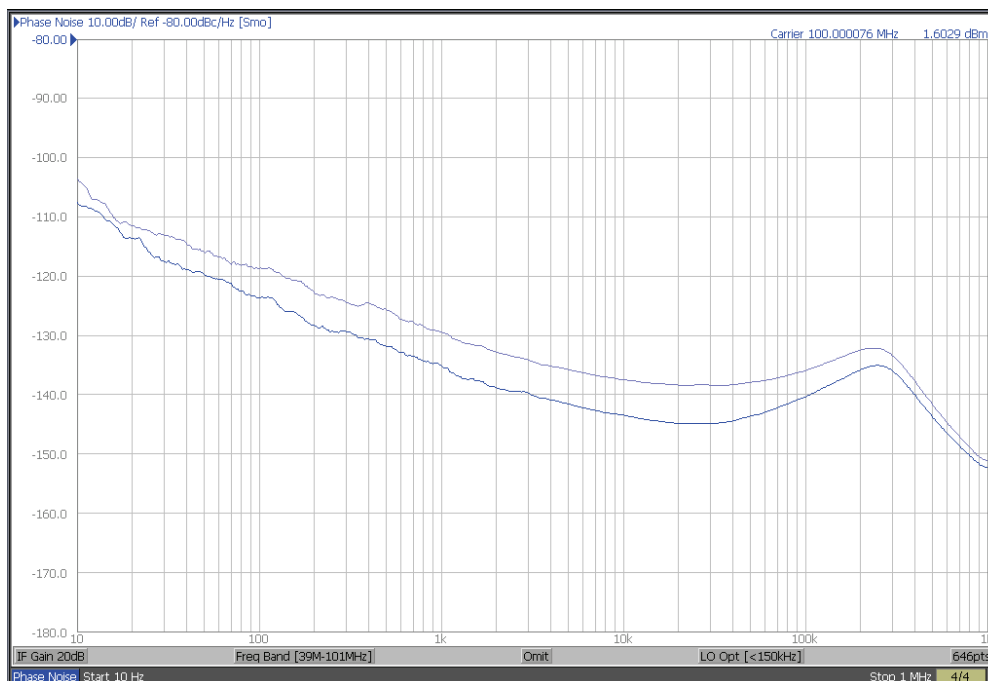


Table 1. Comparative Phase Noise Results of 100 MHz Test Circuit

RF Input Source	F_{IN} (MHz)	F_C (MHz)	N	Phase Noise @ 30 kHz Offset (dBc/Hz)	Normalized Phase Noise Floor (dBc.Hz)
Sine	100	50	2	-138.4	-221.41
Square	100	50	2	-144.8	-227.81

Conclusion

The circuit examples presented demonstrate the limitations of low RF input frequency operation of PLLs. RF signals with slower edge rates can critically degrade phase noise performance due to restrictions of the prescaler. In such cases, increasing the slew rate of the RF signal offers a solution where ultra-low phase noise is required.

Sales Contact and Information

Contact Information:

e2v - <http://www.e2v-us.com> - inquiries@e2v-us.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo and UltraCMOS are registered trademarks, and HaRP is a trademark of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: <http://patents.psemi.com>. All other trademarks and logos are the property of their respective owners.